COMPAL CONFIDENTIAL

MODEL NAME :CAZ30/CAZ40

PCB NO : LA-E112P

BOM P/N : 431A4831L01

Port Map:
Kirkwood Port Map as of 2016-04-01

X8 KBL UMA

Kabylake U

2016-04-20

REV : 0.1 (X00)

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

@EMC@ : EMI, ESD and RF Nopop Component

CXDP@ : XDP Component

CONN@ : Connector Component

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MB PCB

Part Number	Description
DAA000CM000	PCB 1S3 LA-E112P REV0 MB AR 3

Layout Dell logo

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REV:X00
PWB:

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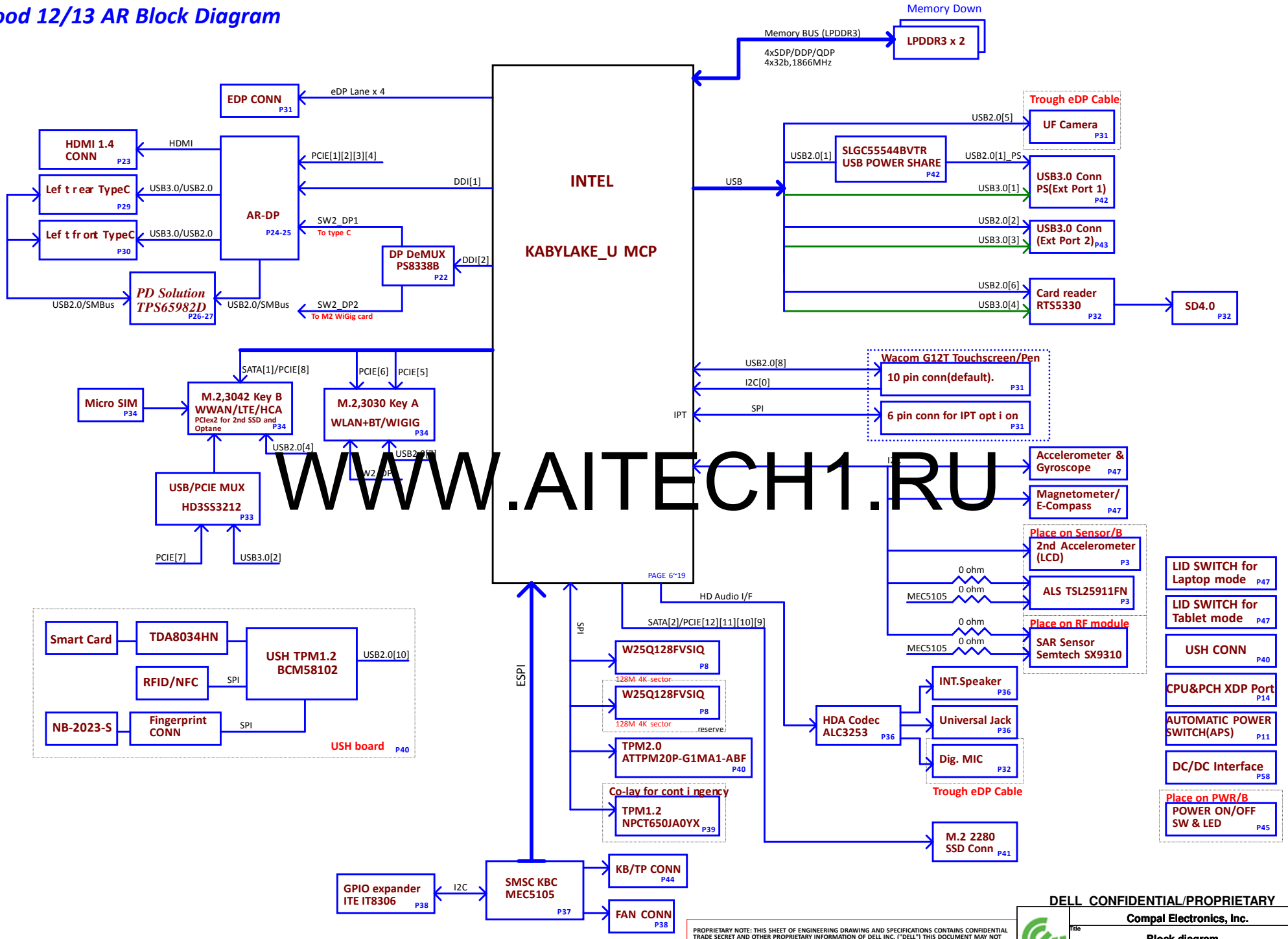
Title	Cover Sheet	
Size	Document Number: LA-E112P	Rev 0.1
Date: Friday, April 22, 2016	Sheet 1 of 58	

Kirkwood 12/13 AR Block Diagram



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Title: Block diagram

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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

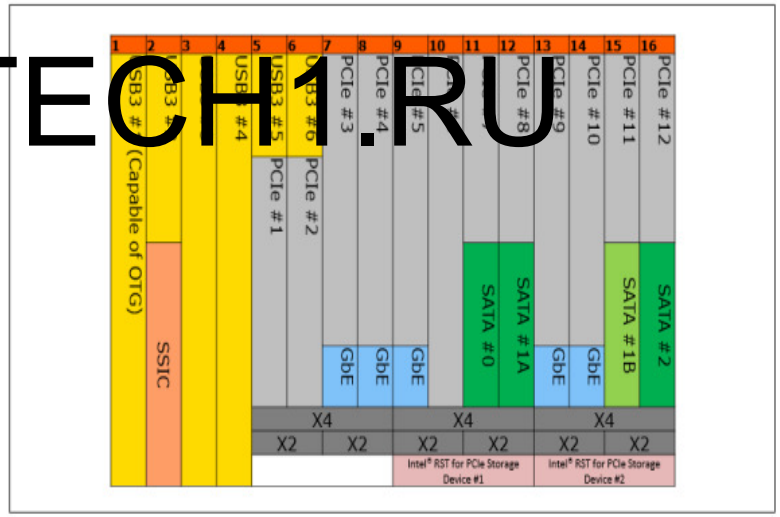
PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_CV2 +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN	+3.3V_M	(M-OFF) +3.3V_M +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB1-->Right
USB3.0-2	SSIC			M.2 3042(LTE)
USB3.0-3				JUSB2-->Lef t
USB3.0-4				SD Card Reader
USB3.0-5		PCIE-1		Alpine Ridge-DP
USB3.0-6		PCIE-2		
		PCIE-3		
		PCIE-4		
		PCIE-5		M.2 3030(WLAN)
		PCIE-6		M.2 3030(WIGIG)
		PCIE-7	SATA-0	M.2 3042(SATA Cache or HCA)
		PCIE-8	SATA-1	
		PCIE-9		M.2 2280 SSD (PCIe4 or SATA)
		PCIE-10		
		PCIE-11	SATA-1*	
		PCIE-12	SATA-2	

USB PORT#	DESTINATION
1	JUSB1-->Right
2	JUSB2-->Lef t
3	NA
4	M2 3042(WWAN)
5	UF Camera
6	SD Card Reader
7	M.2 3030(BT)
8	Touch Screen
9	NA
10	USH

High Speed I/O (HSIO) Lane Multiplexing in KBL U



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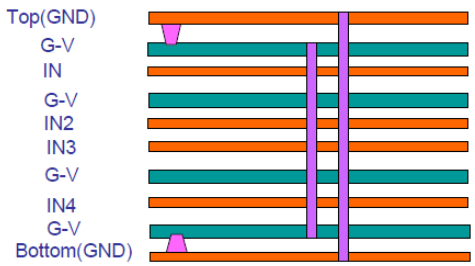
Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	IT-158	0.50000
1	Top(GND)		Copper foil + plating	0.33oz+plating	1.40000
		3.8	Prepreg	1080 or 1086	2.80
2	VCC/GND		Copper foil + plating	0.33oz+plating	1.20000
		4.2	Prepreg	1080 or 1086	2.90
3	IN1		Copper foil	0.5 oz	0.65000
		4.1	CORE	3mil	3.00000
4	VCC/GND		Copper foil	0.5 oz	0.65000
		3.6	Prepreg	1080	3.00
5	IN2		Copper foil	1.0 oz	1.35000
		3.6	CORE	5mil	5.00000
6	IN3		Copper foil	1.0 oz	1.35000
		3.6	Prepreg	1080	3.00
7	VCC/GND		Copper foil	0.5 oz	0.65000
		4.1	CORE	3mil	3.00000
8	IN4		Copper foil	0.5 oz	0.65000
		4.2	Prepreg	1080 or 1086	2.90
9	VCC/GND		Copper foil + plating	0.33oz+plating	1.20000
		3.8	Prepreg	1080 or 1086	2.80
10	Bottom(GND)		Copper foil + plating	0.33oz+plating	1.40000
			SolderMask		
Overall Thickness (1.0mm ± 10%)			39.37		39.40000
					1.00076



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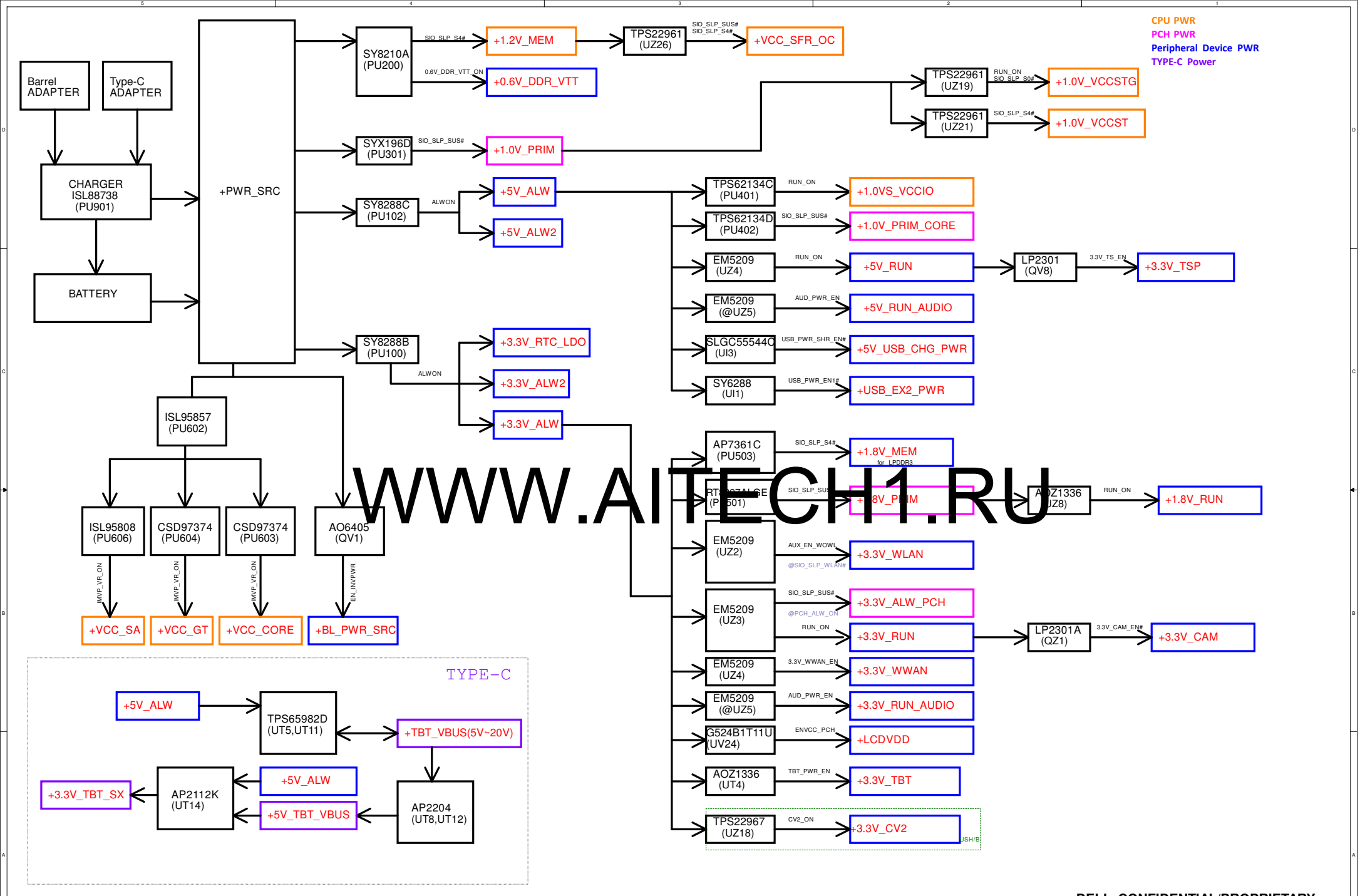
Title: Port assignment

Size | Document Number: LA-E112P | Rev 0.1

Date: Friday, April 22, 2016 | Sheet 3 of 58



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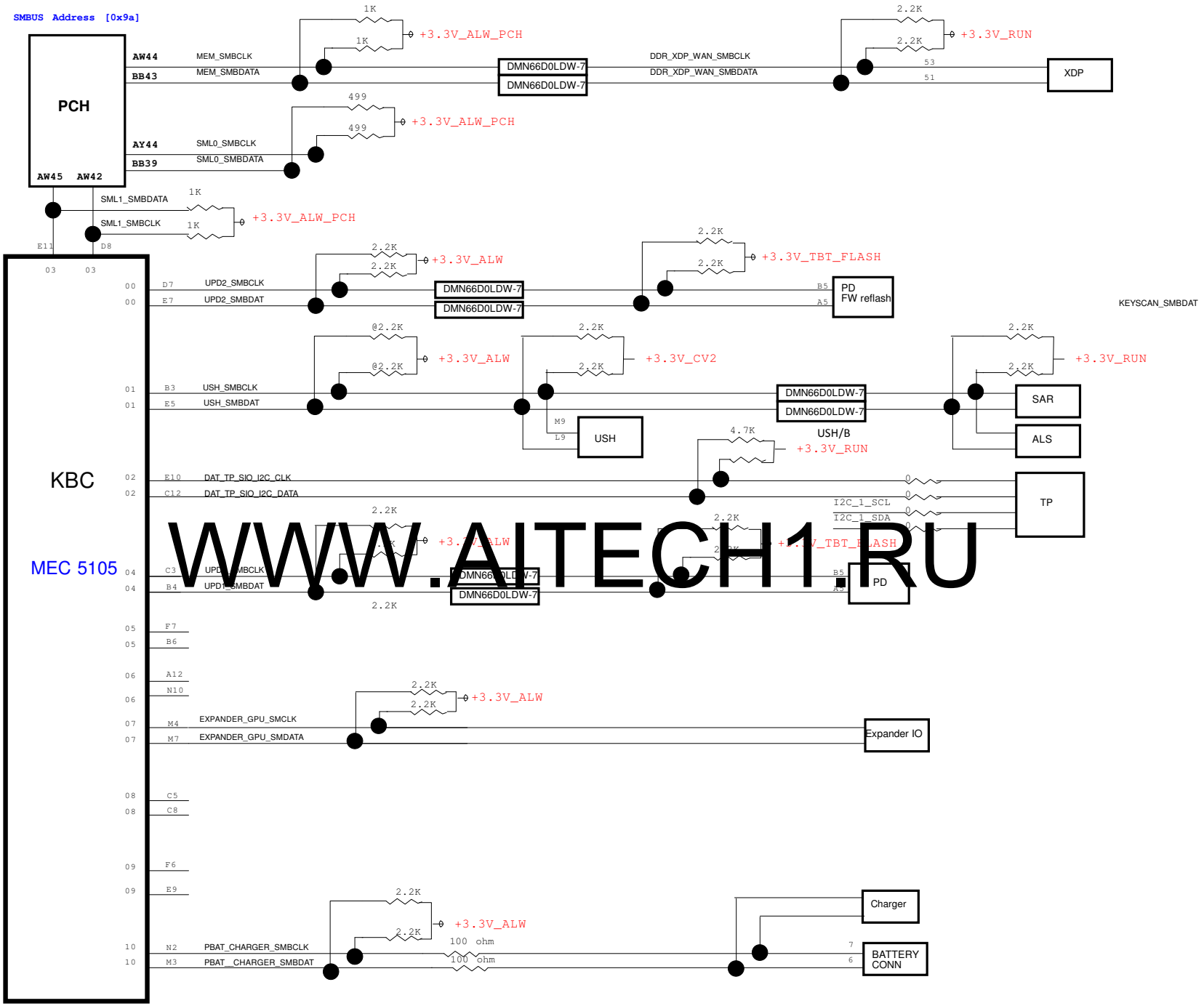
Title: Power rails

Size | Document Number: LA-XXXXP | Rev 0.1

Date: Friday, April 22, 2016 | Sheet 4 of 58



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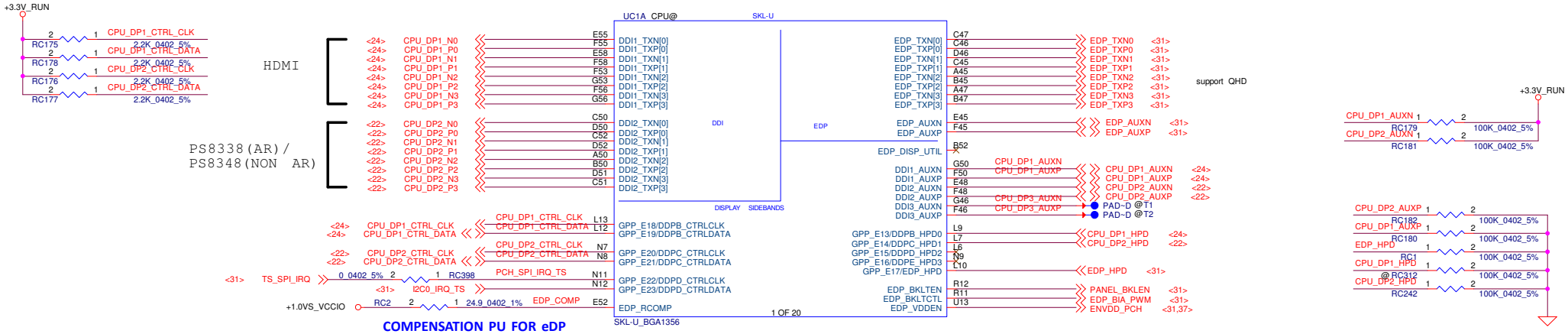

COMPENSATION PU FOR eDP

CAD Note:Trace width=20 mils ,Spacing=25mil, Max length=100 mils.

SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0

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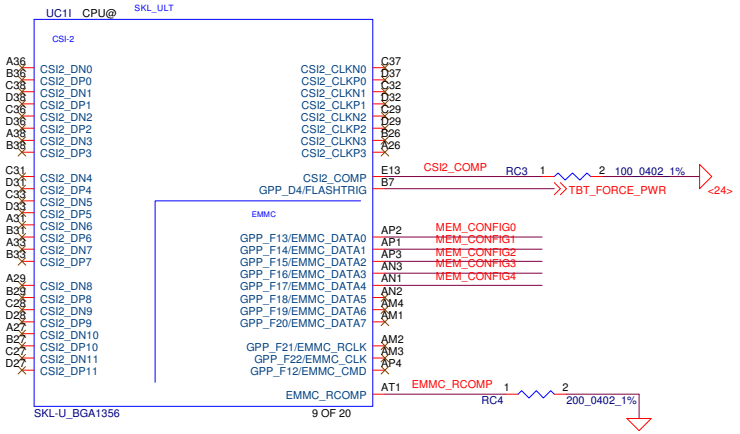
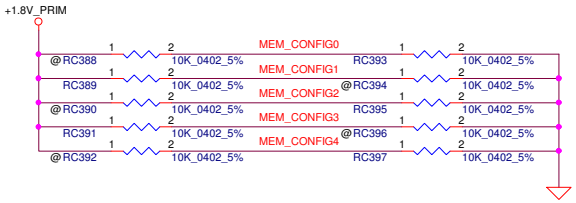
GPIO PIN	PIN NAME	SPEED	Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_D5	MEM_CONFIG0	1600 Mbps	0	0	0	0	0	1	0	1	0
GPP_D6	MEM_CONFIG1		0	0	0	1	0	0	1	1	0
GPP_D7	MEM_CONFIG2		0	0	0	0	1	1	1	1	0
GPP_D8	MEM_CONFIG3		0	0	0	0	0	0	0	0	1
GPP_D9	MEM_CONFIG4		0	0	0	0	0	0	0	0	0

GPIO PIN	PIN NAME	SPEED	Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_D5	MEM_CONFIG0	1866 Mbps	1	0	1	0	1	0	1	0	1
GPP_D6	MEM_CONFIG1		0	1	1	0	0	1	1	0	0
GPP_D7	MEM_CONFIG2		0	0	0	1	1	1	1	0	0
GPP_D8	MEM_CONFIG3		1	1	1	1	1	1	1	0	0
GPP_D9	MEM_CONFIG4		0	0	0	0	0	0	0	1	1

GPIO PIN	PIN NAME	SPEED	Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_D5	MEM_CONFIG0	2133 Mbps (UI)	0	1	0	1	0	1	0	1	0
GPP_D6	MEM_CONFIG1		1	1	0	0	1	1	0	0	1
GPP_D7	MEM_CONFIG2		0	0	1	1	1	1	0	0	0
GPP_D8	MEM_CONFIG3		0	0	0	0	0	0	1	1	1
GPP_D9	MEM_CONFIG4		1	1	1	1	1	1	1	1	1





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For LPDDR3

LPDDR3, Ballout for side by side(Non-Interleave)

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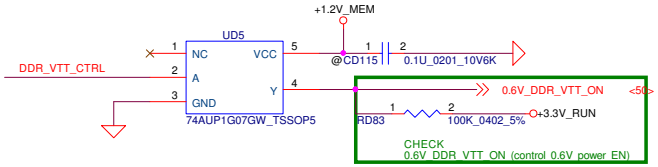
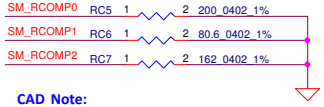


LPDDR3 COMPENSATION SIGNALS



CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

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Title: CPU (2/14)

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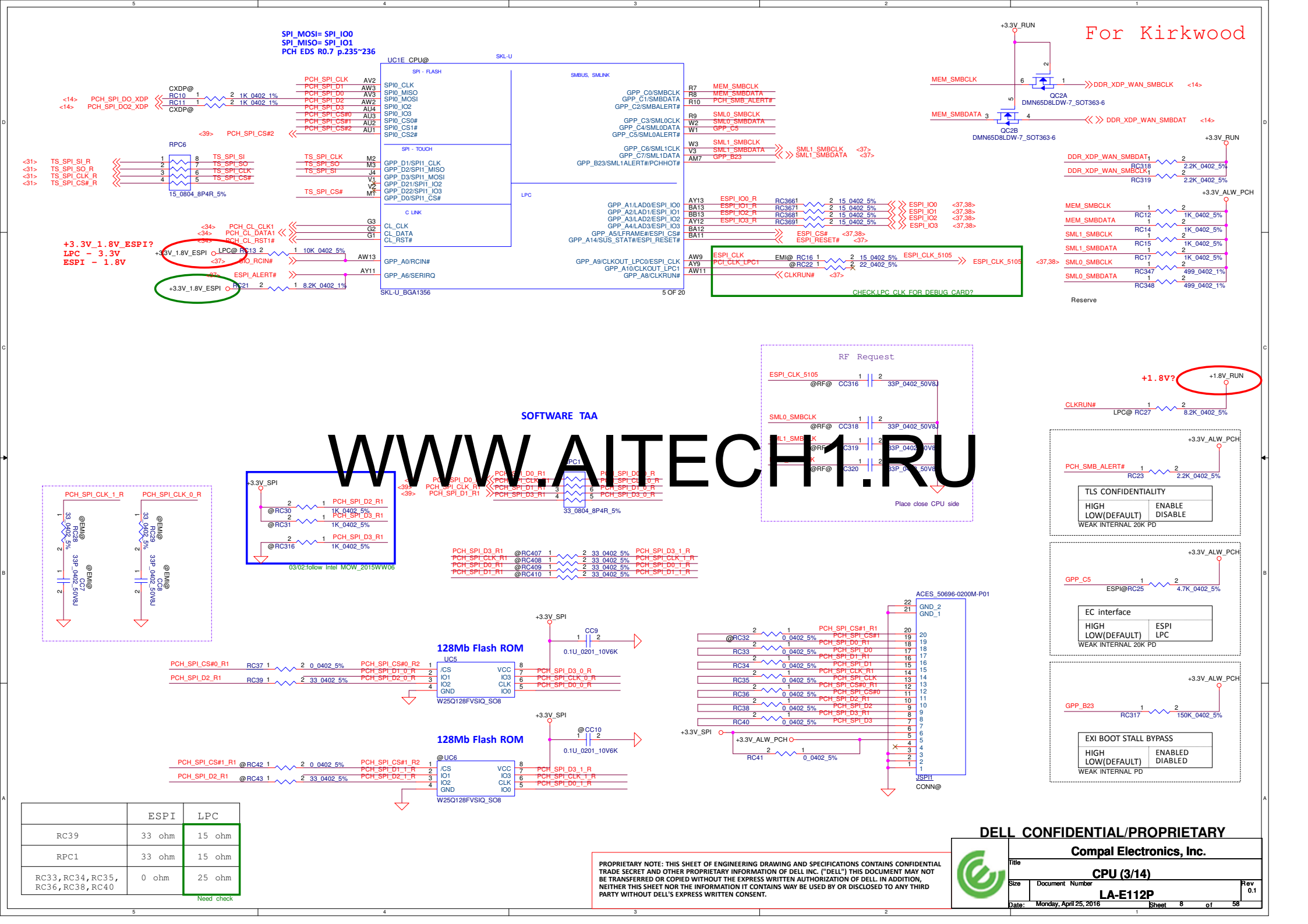

	ESPI	LPC
RC39	33 ohm	15 ohm
RPC1	33 ohm	15 ohm
RC33,RC34,RC35, RC36,RC38,RC40	0 ohm	25 ohm

Need check

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Title: CPU (3/14)

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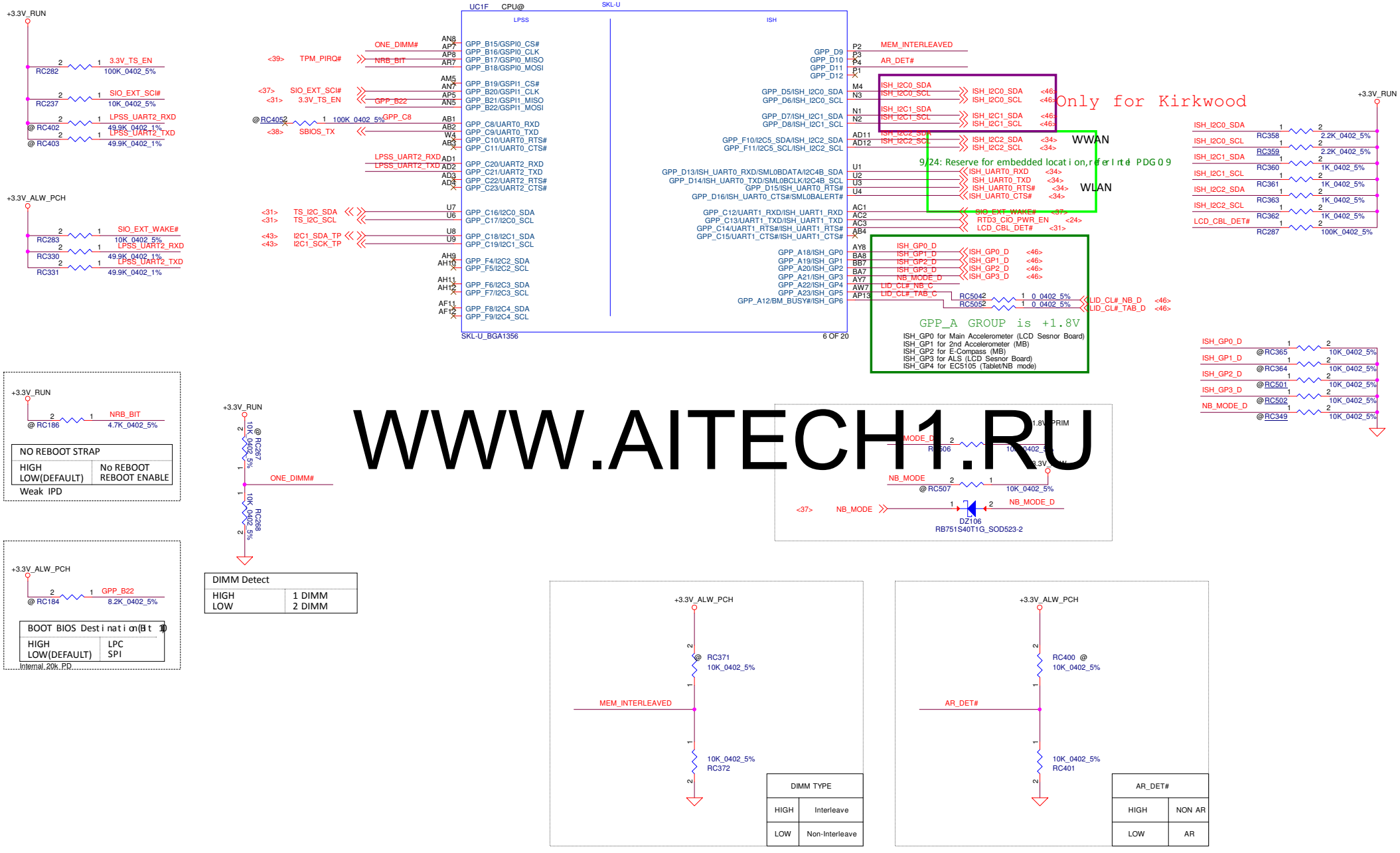

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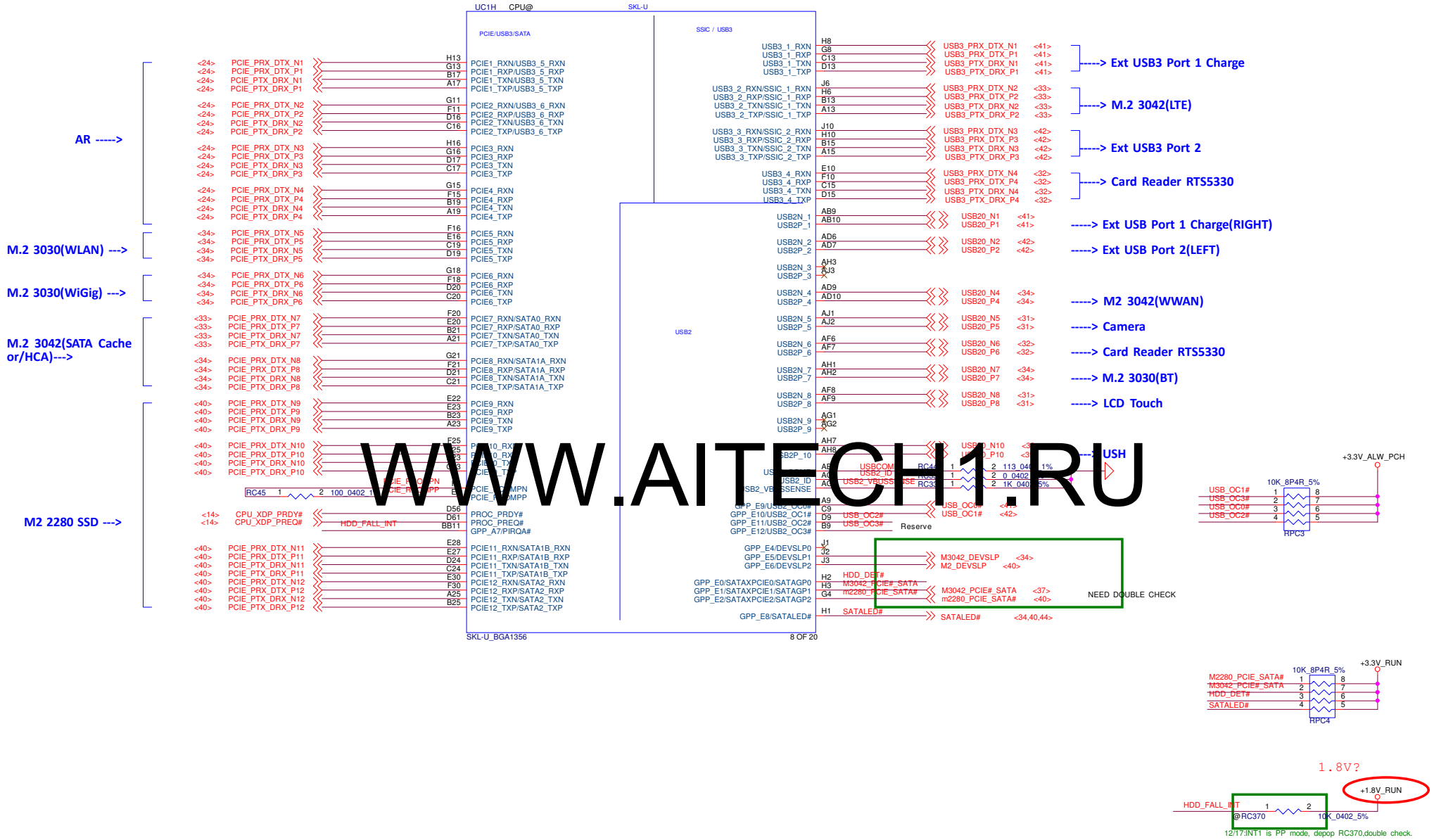
For AR, Kirkwood



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1.8V?

12/17:INT1 is PP mode, depop RC370,double check.

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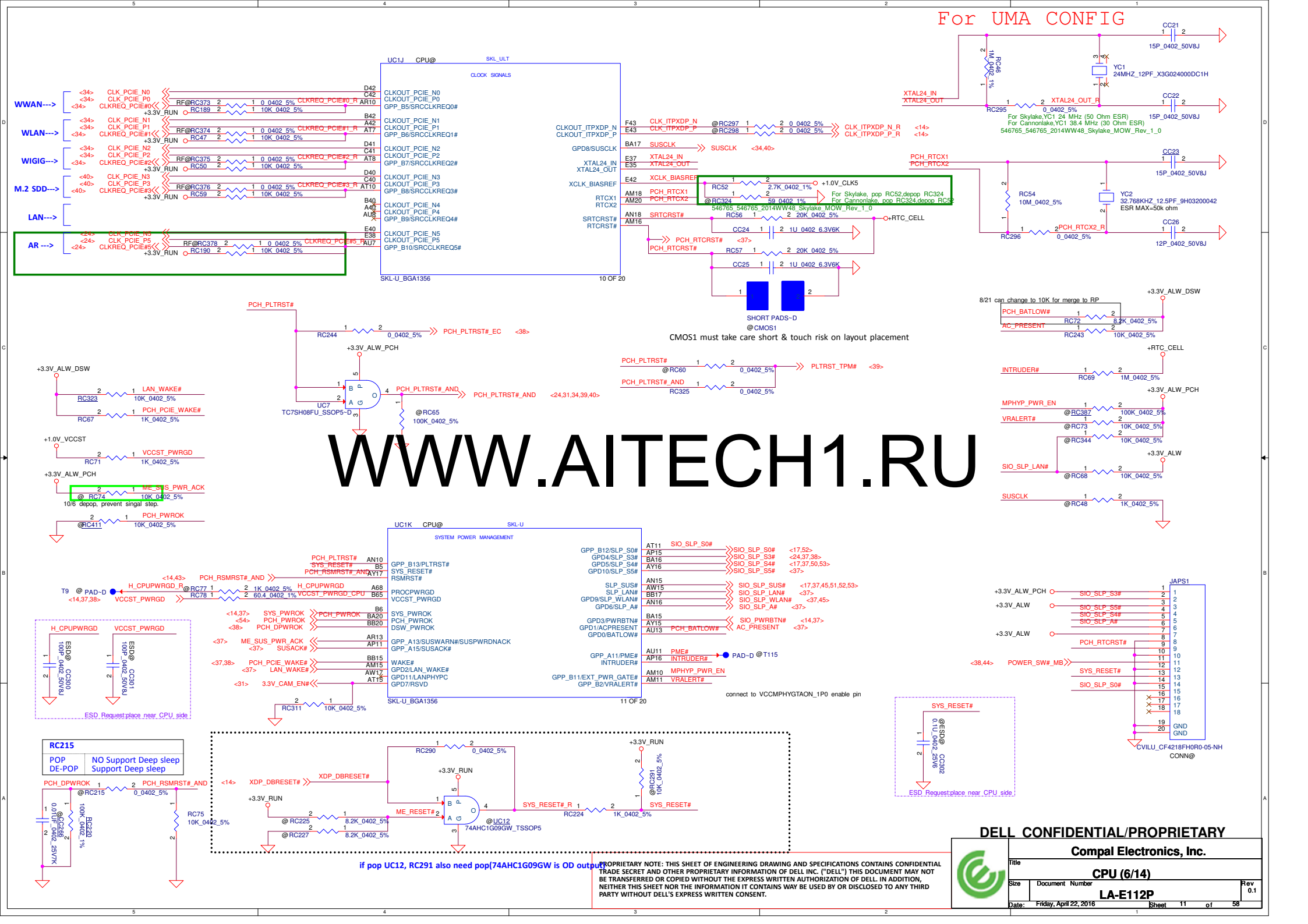
For UMA CONFIG



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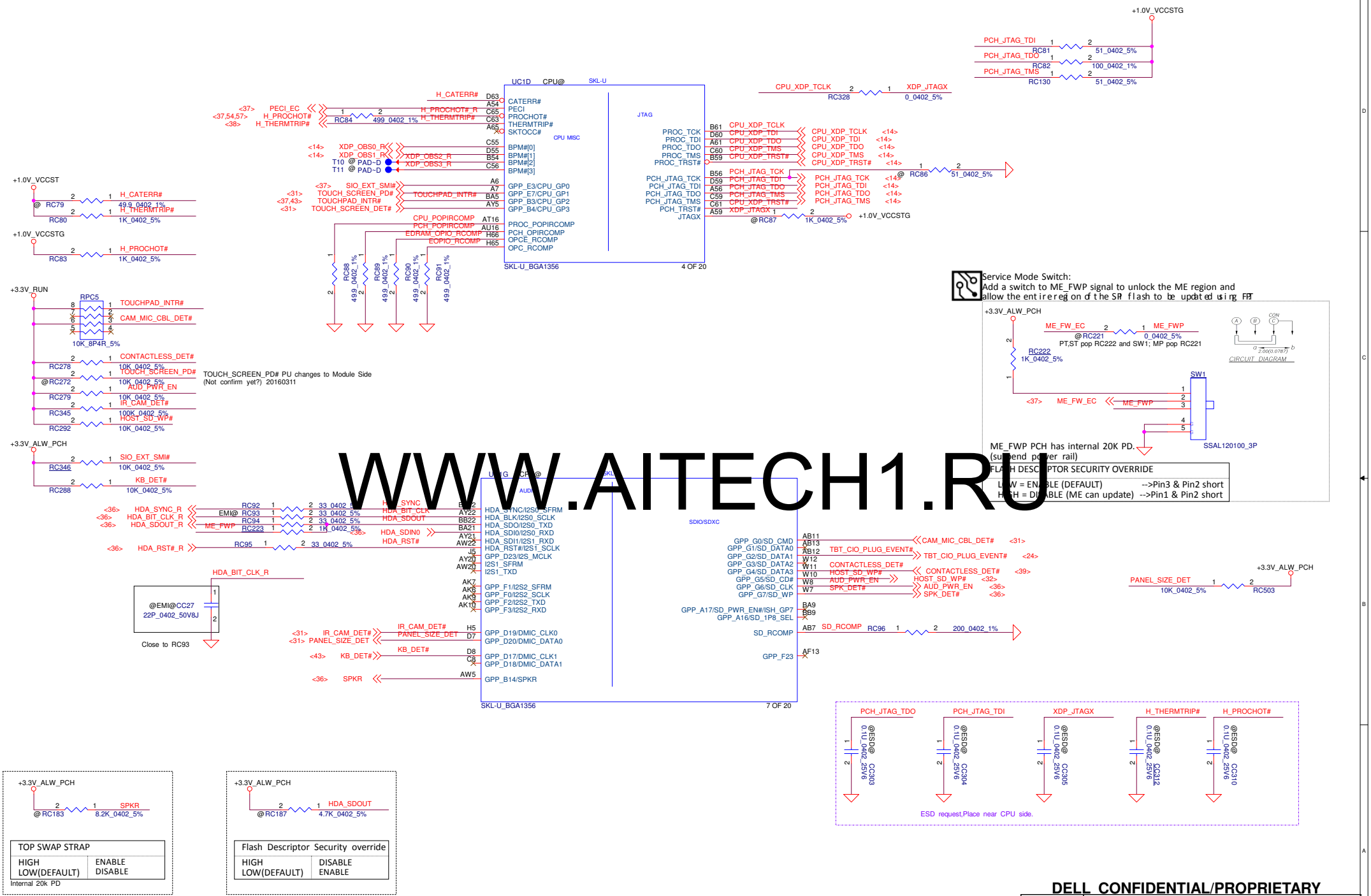

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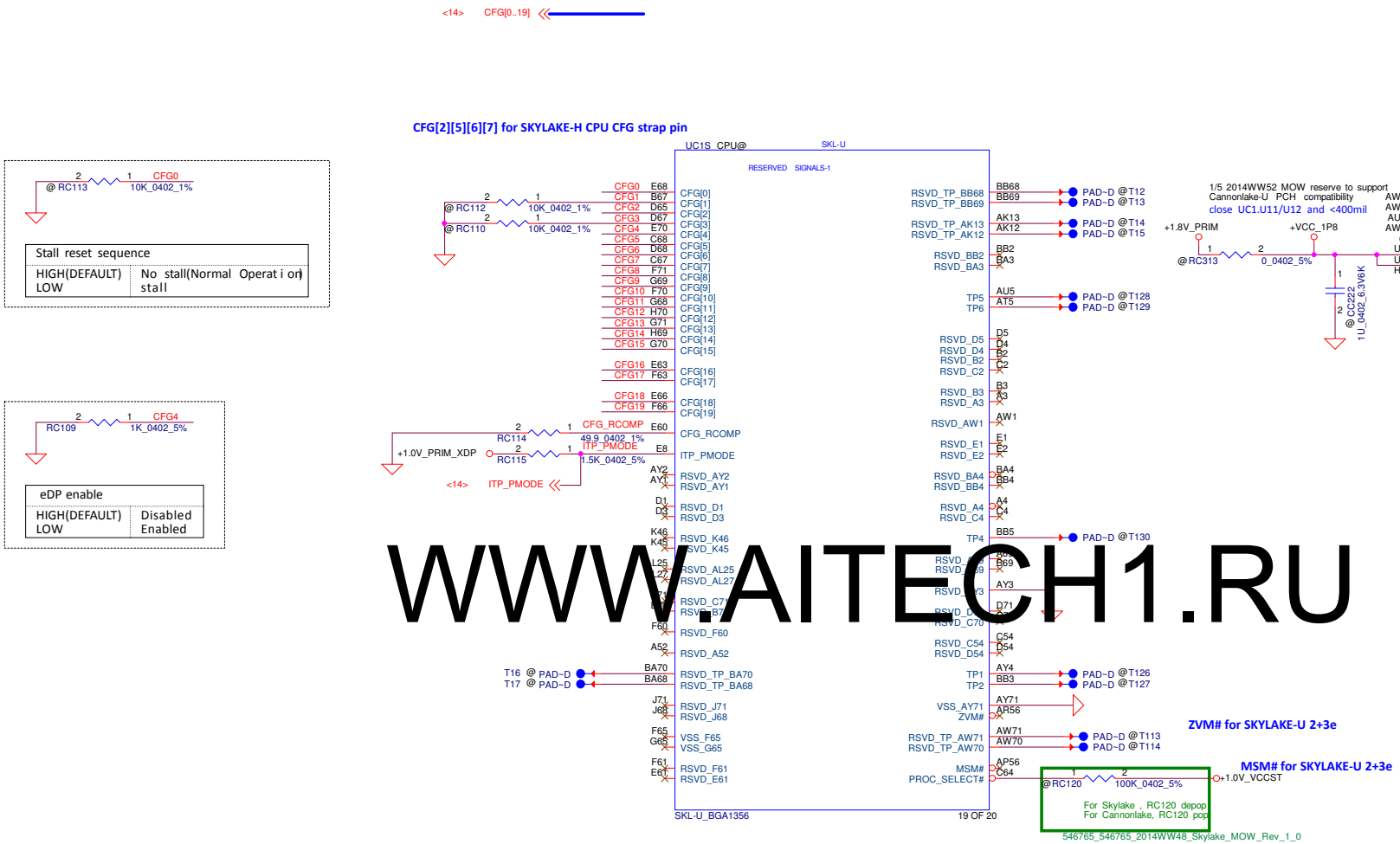

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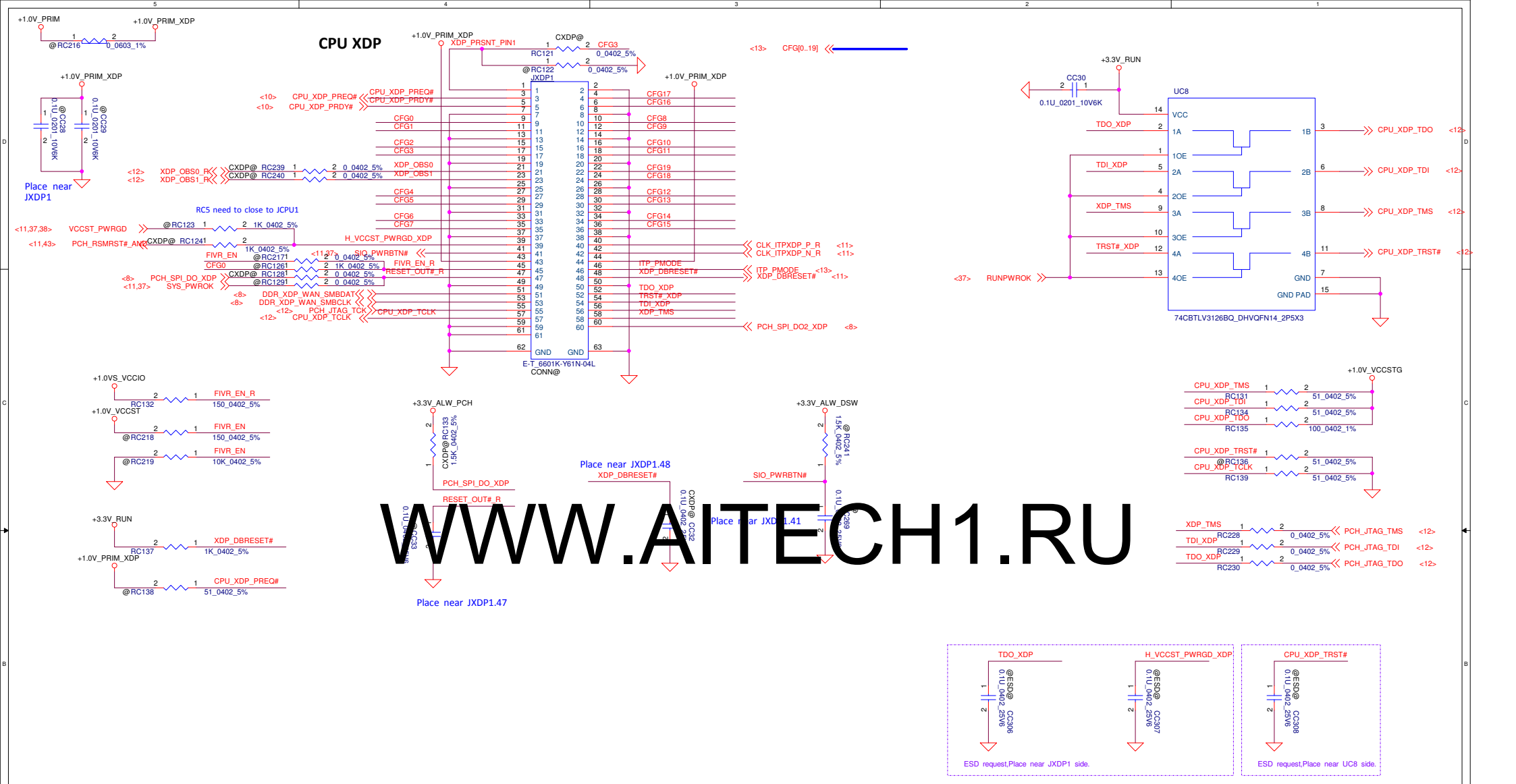

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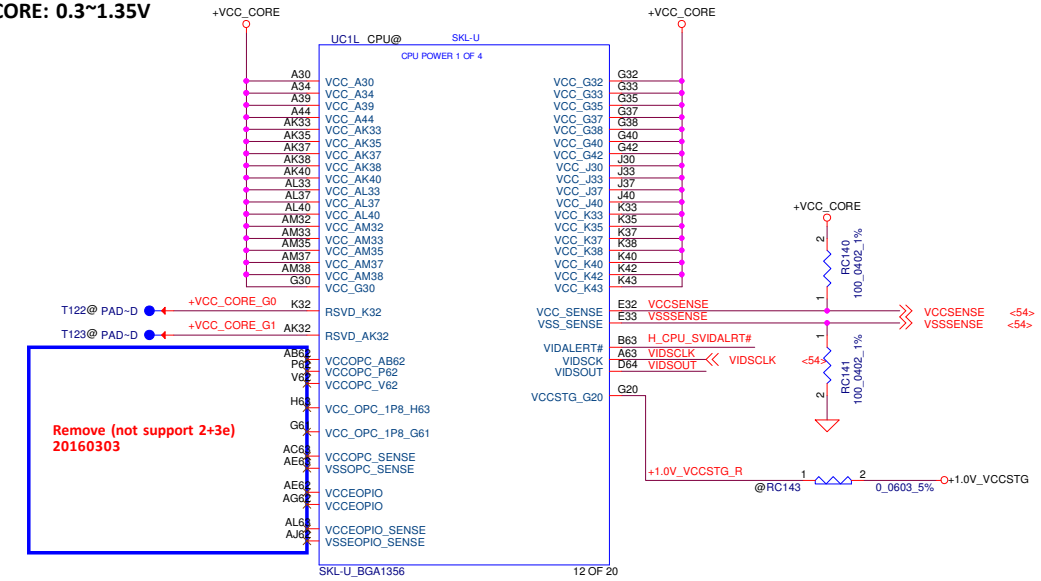
+VCC_CORE: 0.3~1.35V

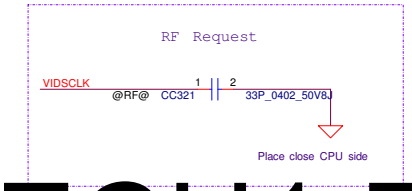
PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source



Remove (not support 2+3e)
20160303

VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e
(w/ on package cache)



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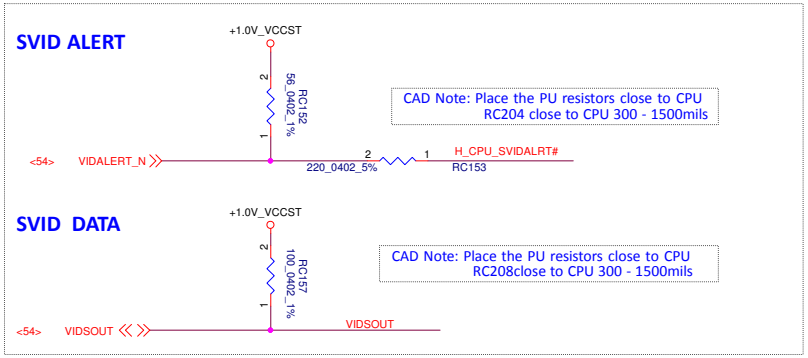

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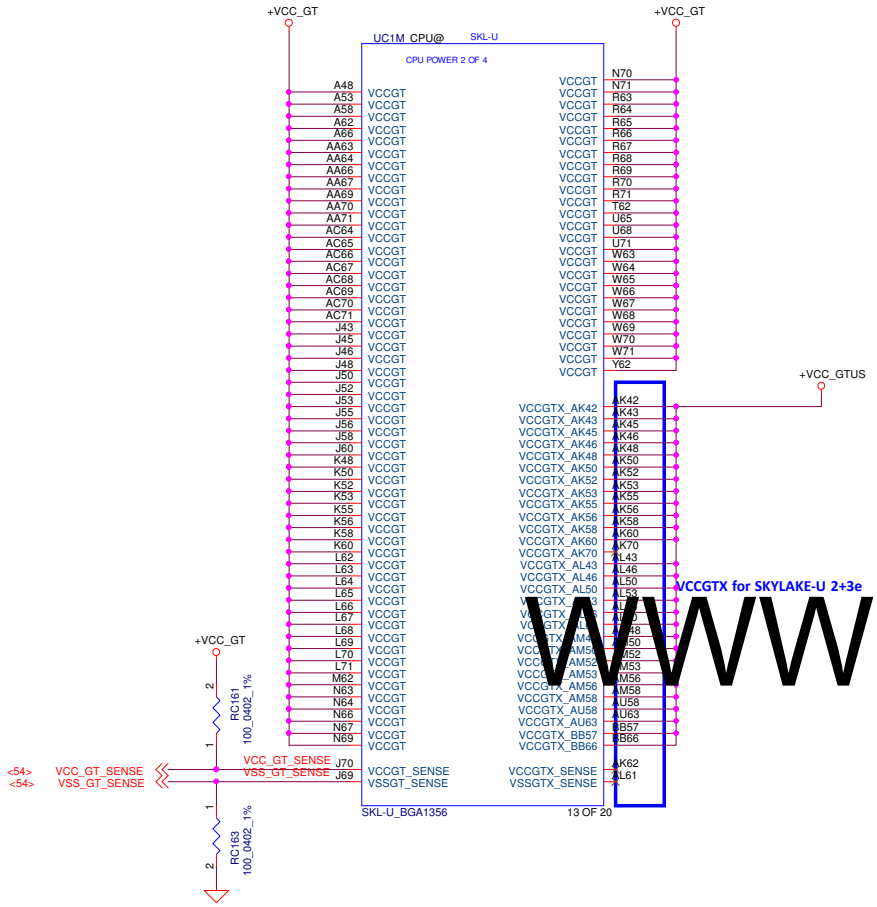
Compal Electronics, Inc.

Title: CPU (10/14)

Size: | Document Number: LA-E112P | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 15 of 58

+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V



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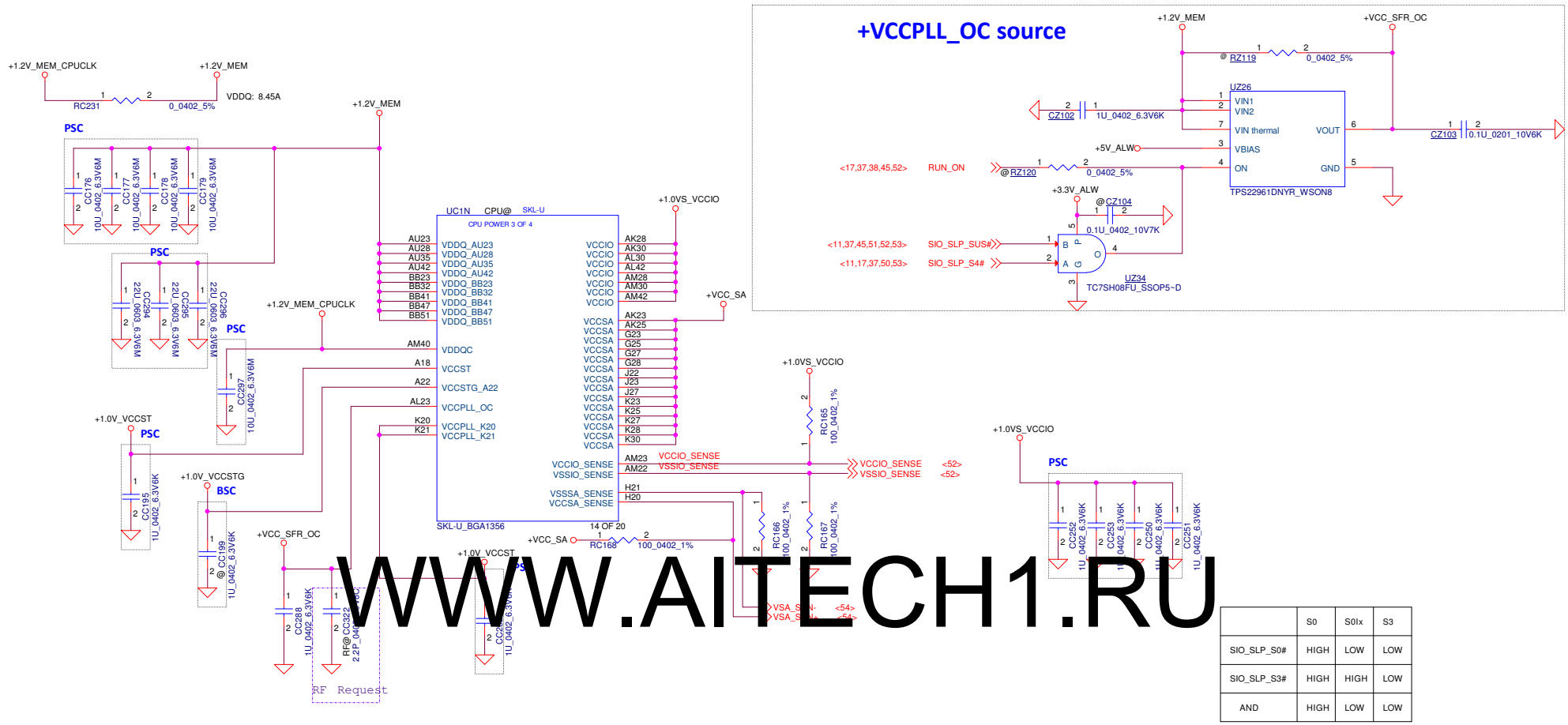
Compal Electronics, Inc.	
Title	CPU (11/14)
Size / Document Number	LA-E112P
Rev	0.1
Date: Friday, April 22, 2016	Sheet 16 of 58



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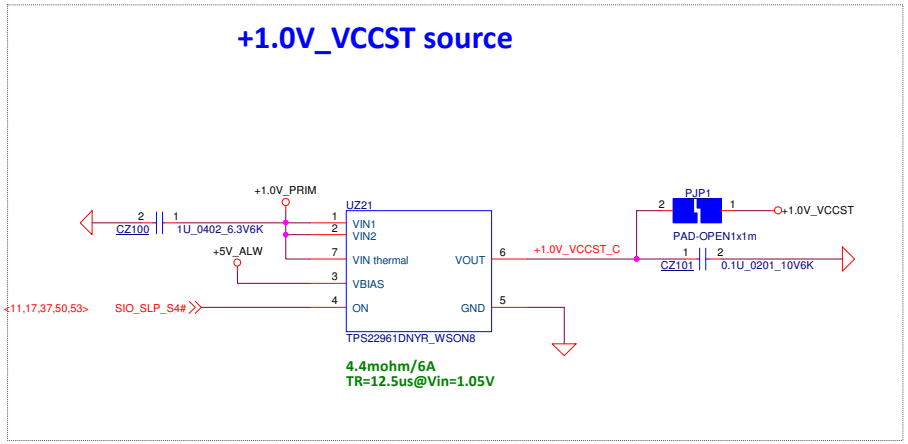
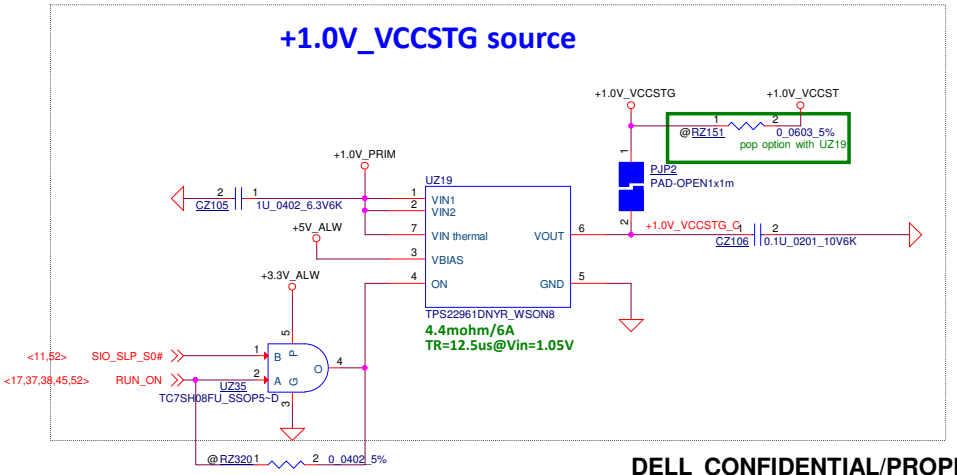
	S0	S0Ix	S3
SIO_SLP_S0#	HIGH	LOW	LOW
SIO_SLP_S3#	HIGH	HIGH	LOW
AND	HIGH	LOW	LOW





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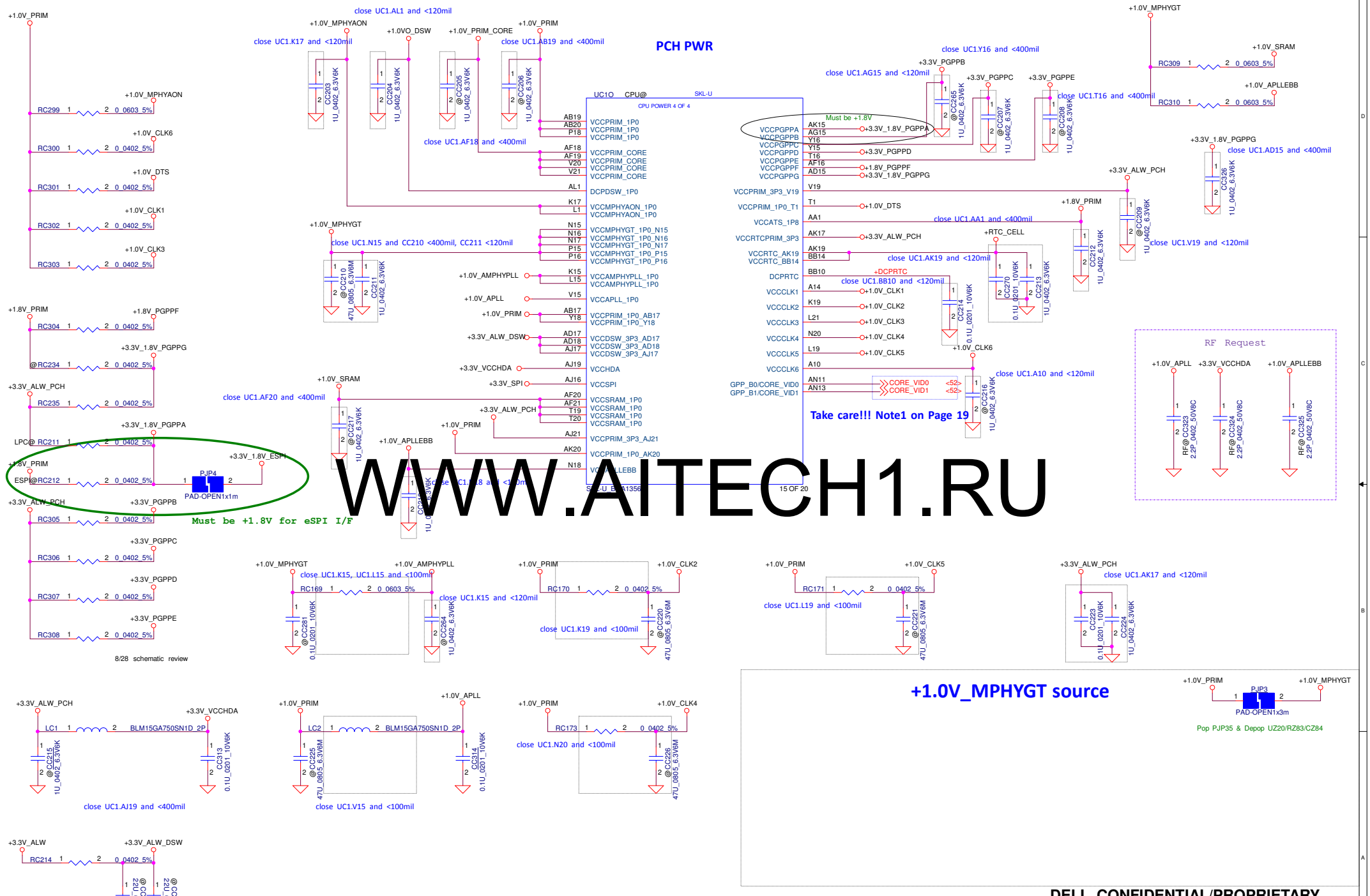
Compal Electronics, Inc.

Title: CPU (12/14)

Size | Document Number: LA-E112P | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 17 of 58



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Compal Electronics, Inc.

Title: CPU (13/14)

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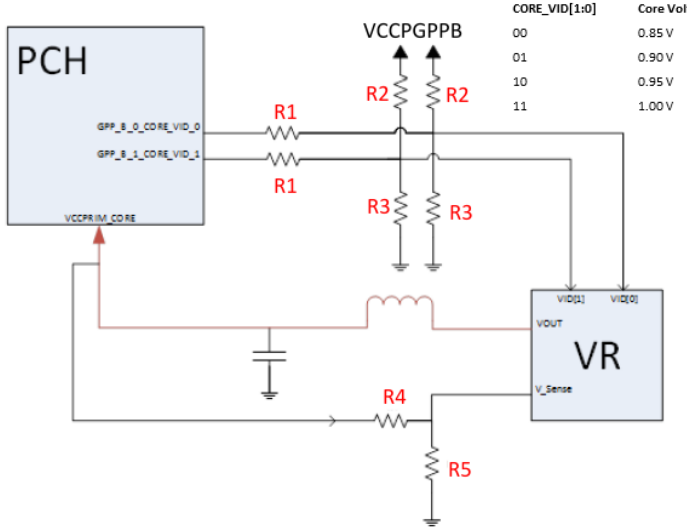
Date: Friday, April 22, 2016 | Sheet 18 of 58

Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



CORE_VID[1:0]	Core Voltage ID
00	0.85 V
01	0.90 V
10	0.95 V
11	1.00 V

For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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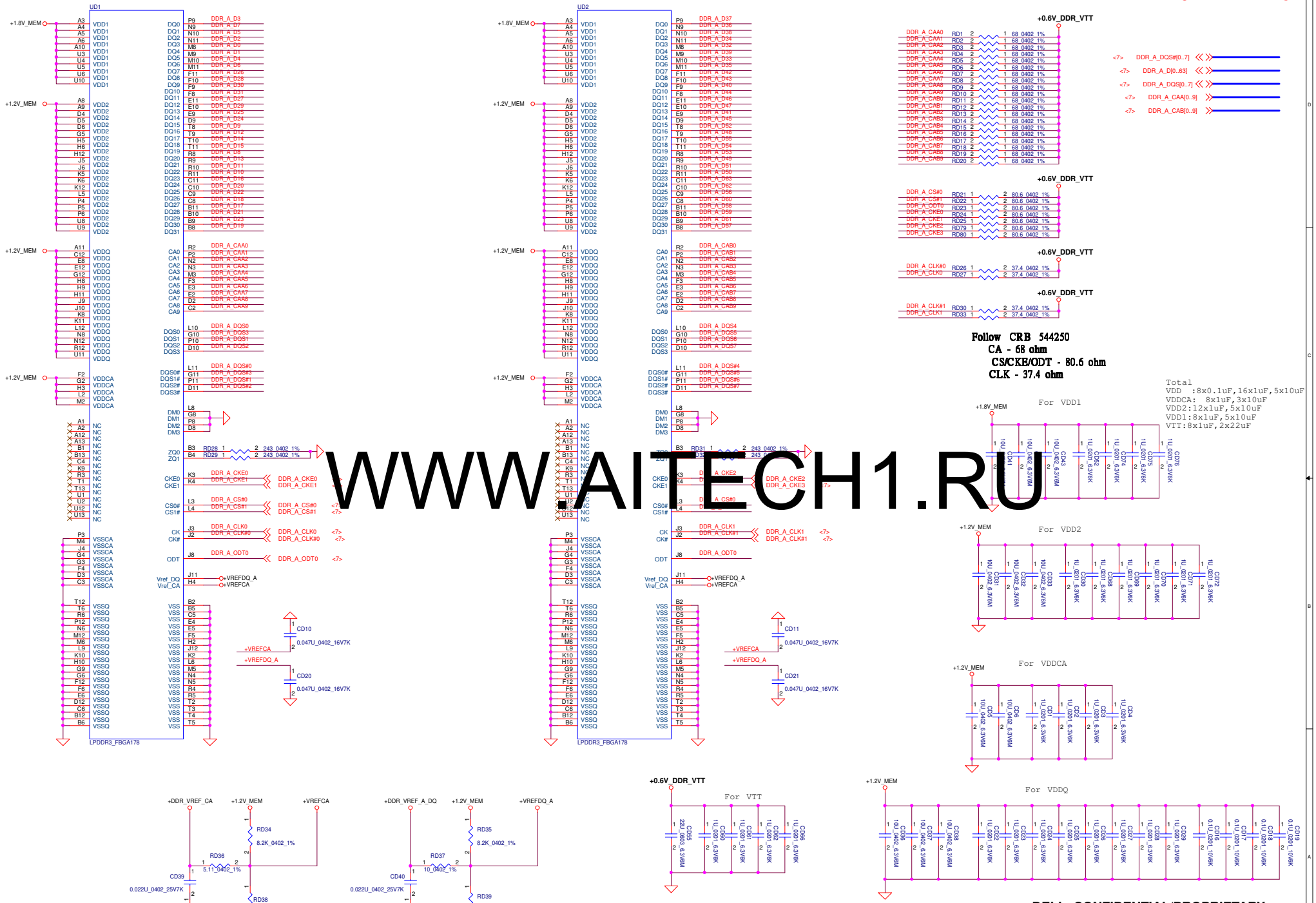
For LPDDR3



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Compal Electronics, Inc.

Title: LPDDR3

Size | Document Number: LA-E112P | Rev: 0.1

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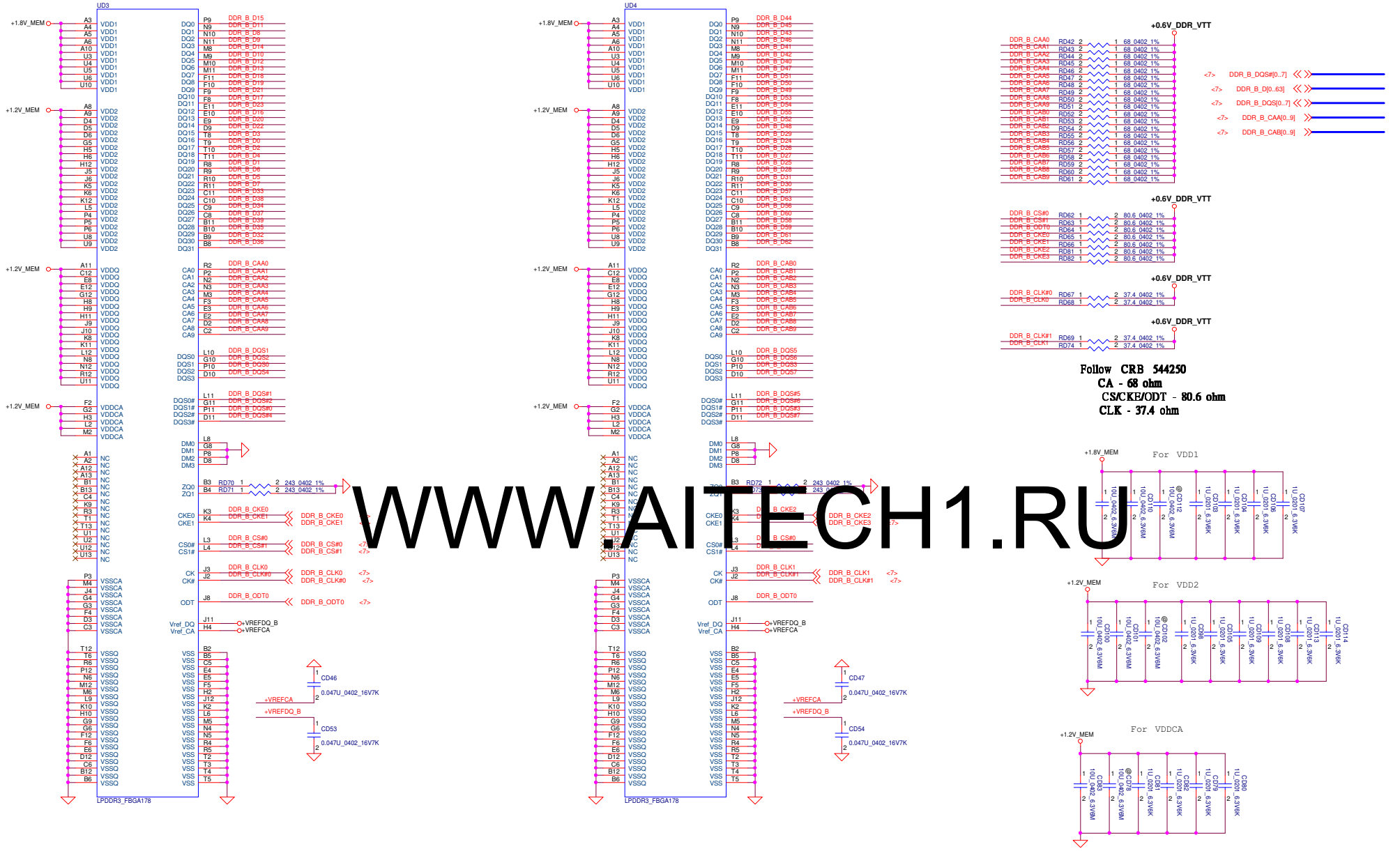
For LPDDR3



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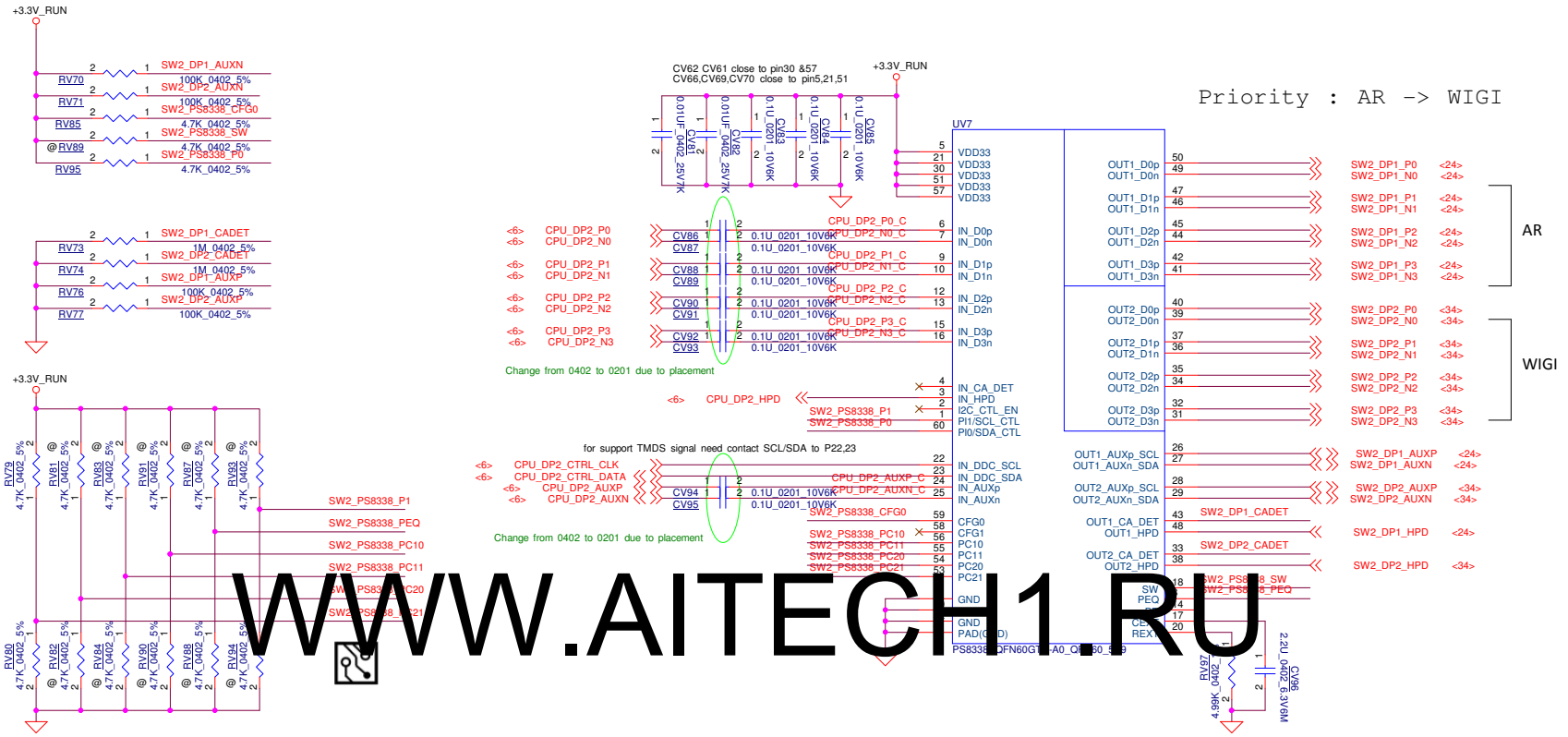
Title	LPDDR3		
Size	Document Number	LA-E112P	Rev 0.1
Date: Friday, April 22, 2016	Sheet 21 of 58		

For Steamboat12/14 &Kirkwood



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Port switching control or priority configuration. Internal pull down ~150KΩ , 3.3V I/O
For Control Switching Mode (CFG0 = L):
SW = L: Port1 is selected (default)
SW = H: Port2 is selected
For Automatic Switching Mode (CFG0 = H):
~~SW = L: Port1 has higher priority when both ports are plugged (default)~~
SW = H: Port2 has higher priority when both ports are plugged

vender sugguest MUX use LLEQ PEQ=M and PI0=H !!

Programmable input equalization levels, Internal pull down at ~150Kohm,3.3V I/O
PEQ =
L: default,LEQ, compensate channel loss up to 11.5dB @HBR2
H: HEQ, compensate channel loss up to 14.5dB @HBR2
~~M:LLEQ, compensate channel loss up to 8.5dB @HBR2~~

PI0:Automatic EQ disable, Internal pull down ~150K ohm, 3.3V I/O
PI0 = L: Automatic EQ enable(default)
H: Automatic EQ disable

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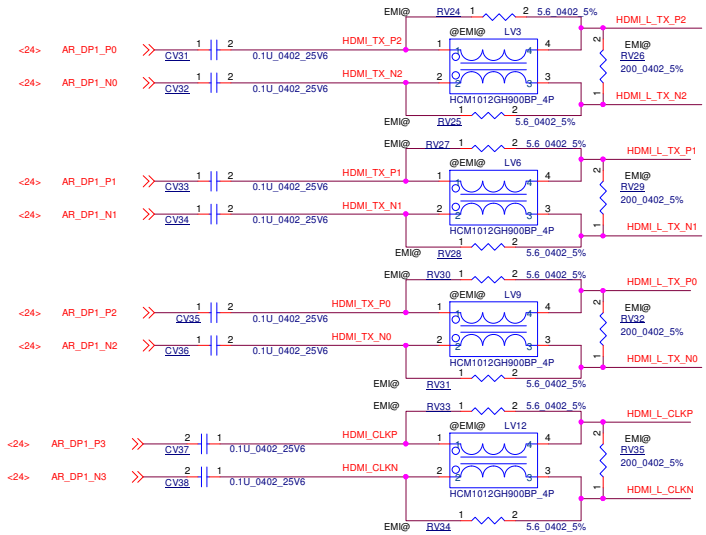
Compal Electronics, Inc.

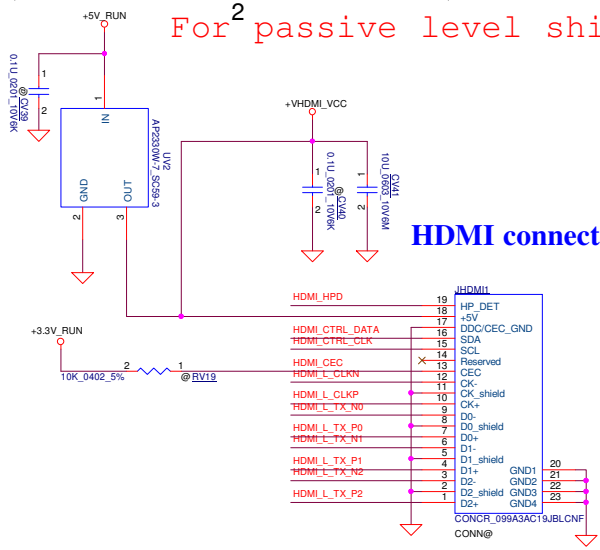
Title: DP SW2 PS8338

Size | Document Number: LA-E112P | Rev 0.1

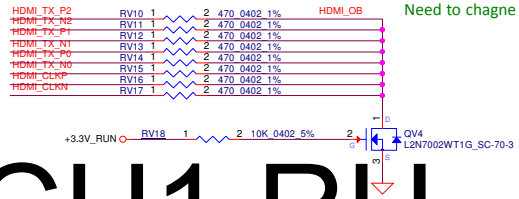
Date: Friday, April 22, 2016 | Sheet 22 of 58

For passive level shifter from AR





LINK CONCR_099A3AC19JBLCNF DONE
20160308
Need to chagne new one and same as DC232003400 (20160315)



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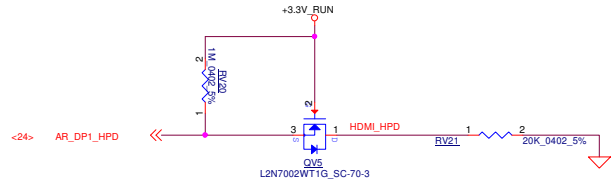

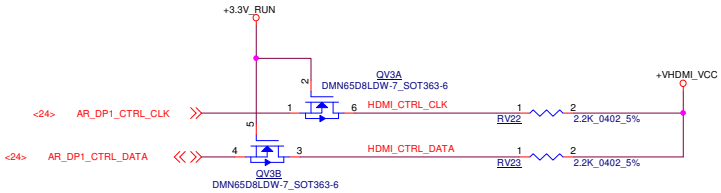

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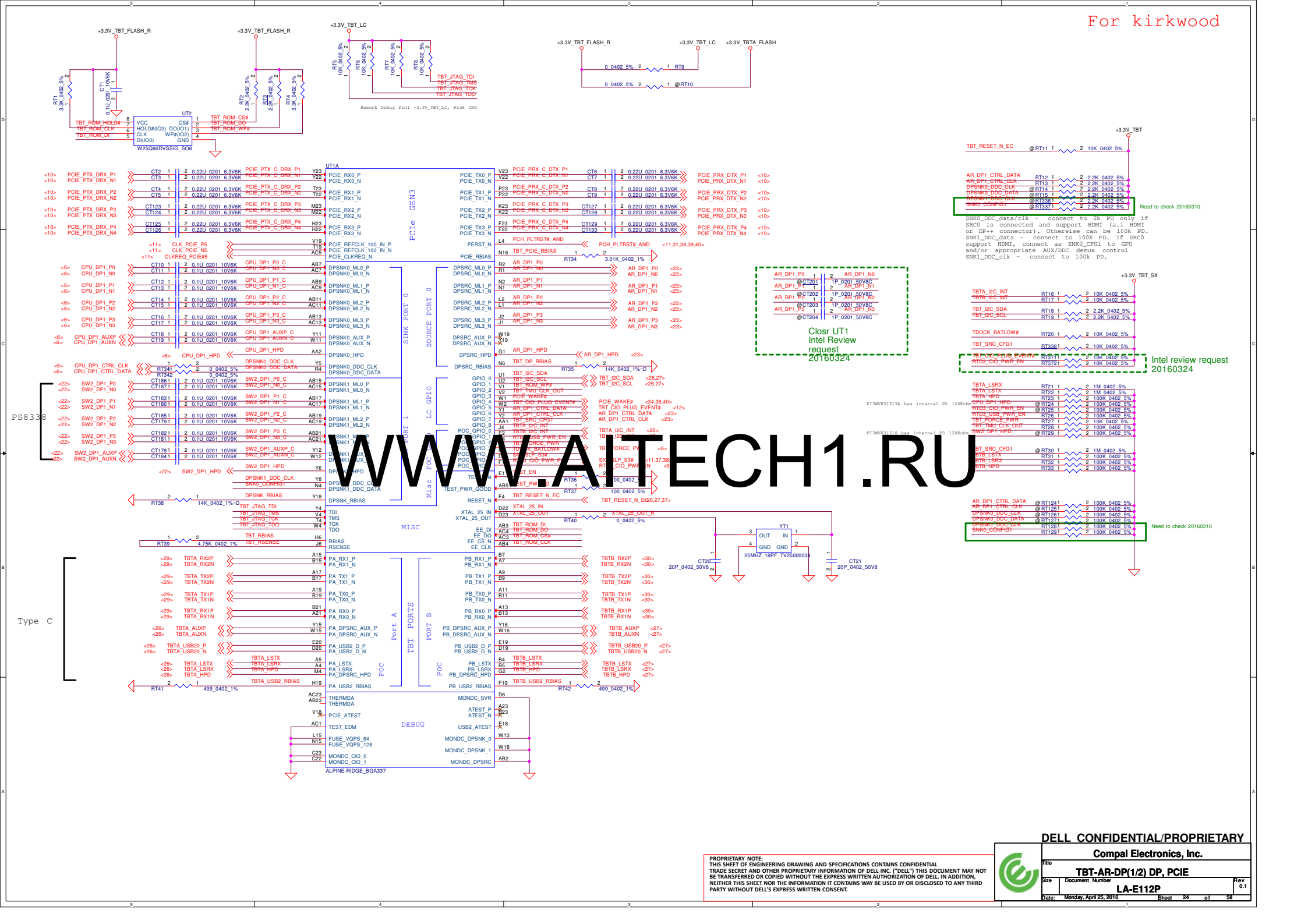
Compal Electronics, Inc.		
Title: HDMI CONN		
Size	Document Number: LA-E112P	Rev: 0.1
Date: Friday, April 22, 2016	Sheet 23 of 58	

For kirkwood



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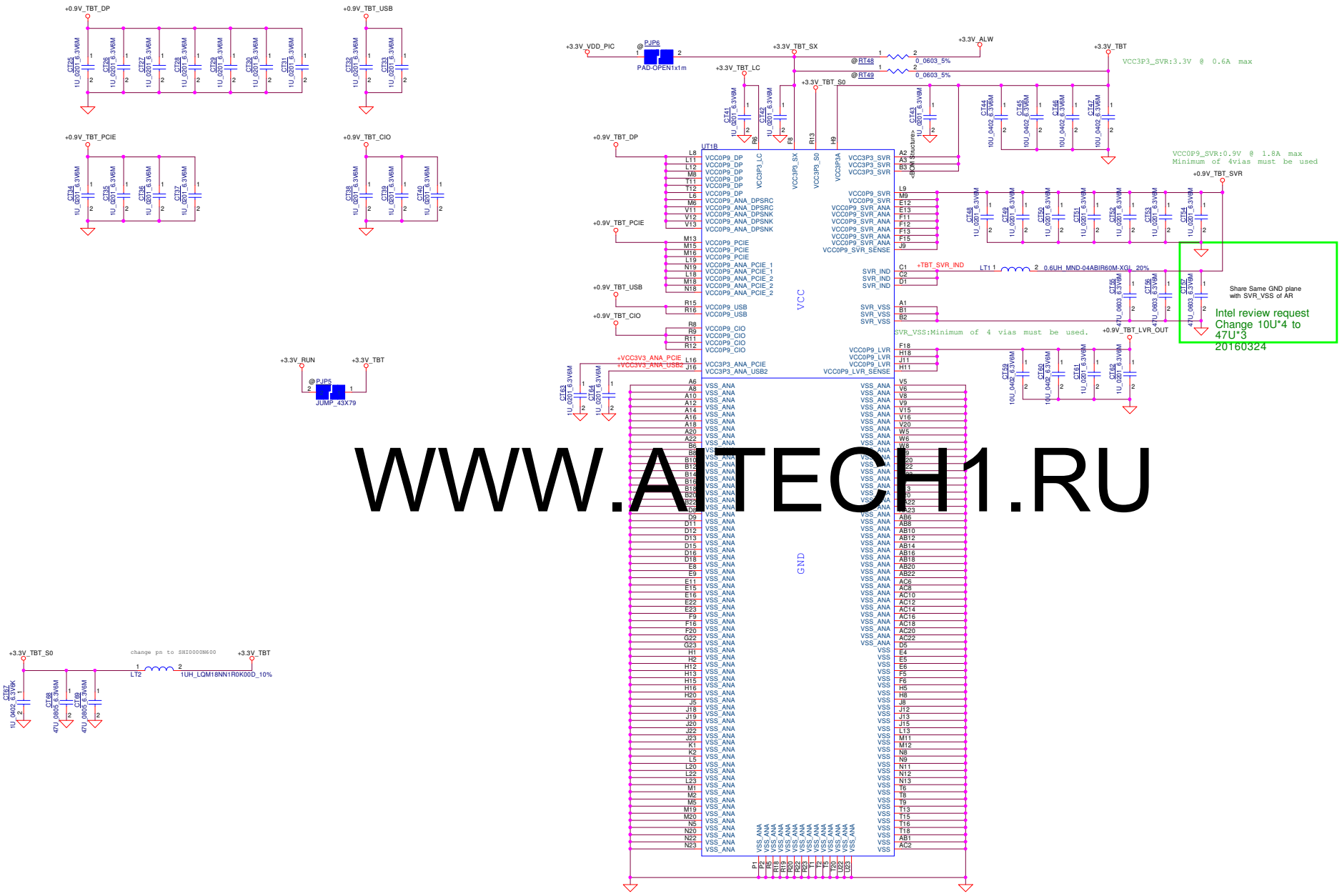
Compal Electronics, Inc.

Title: TBT-AR-DP(1/2) DP, PCIE

Size: | Document Number: LA-E112P | Rev: 0.1

Date: Monday, April 25, 2016 | Sheet 24 of 58

For Steamboat 12/14 &kirkwood,For AR



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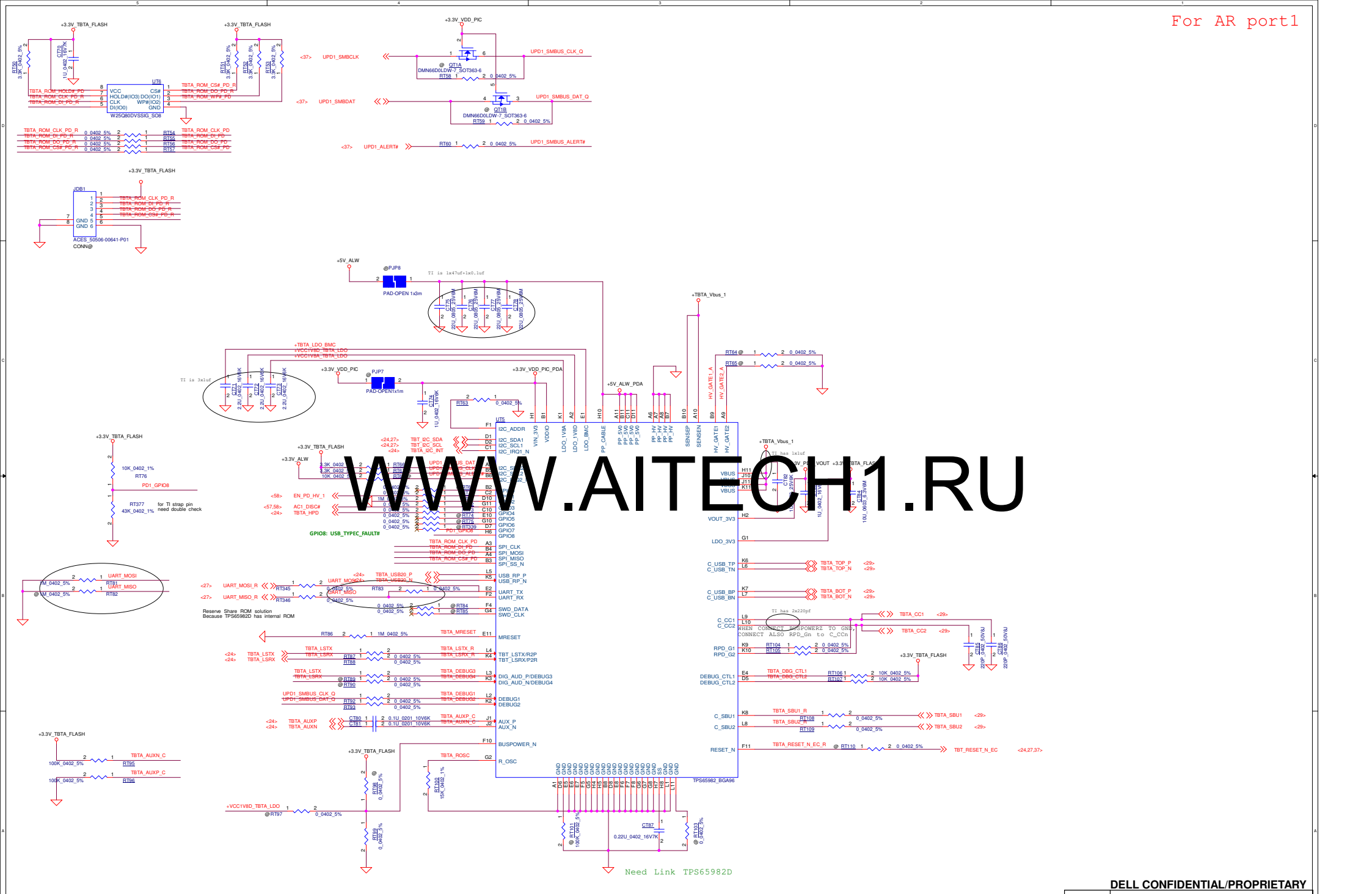
Compal Electronics, Inc.

Title: TBT-AR-SP(2/2) PWR,VSS

Size | Document Number: LA-E112P | Rev: 0.1

Date: Monday, April 25, 2016 | Sheet 25 of 58

For AR port1



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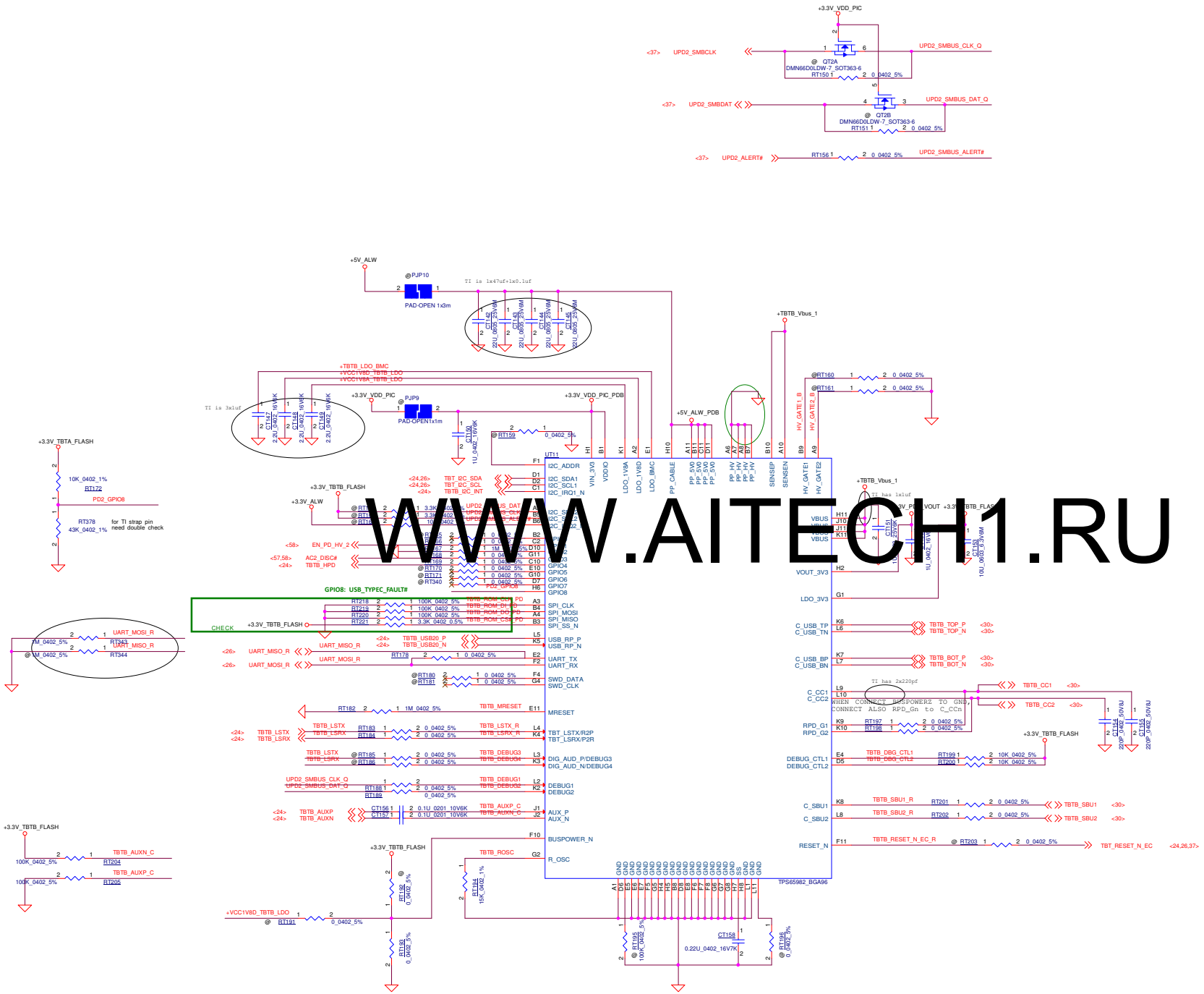
Compal Electronics, Inc.

Title: [Type C]PD Controller TI

Size | Document Number: LA-E112P | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 26 of 58

For AR port2 kirkwood



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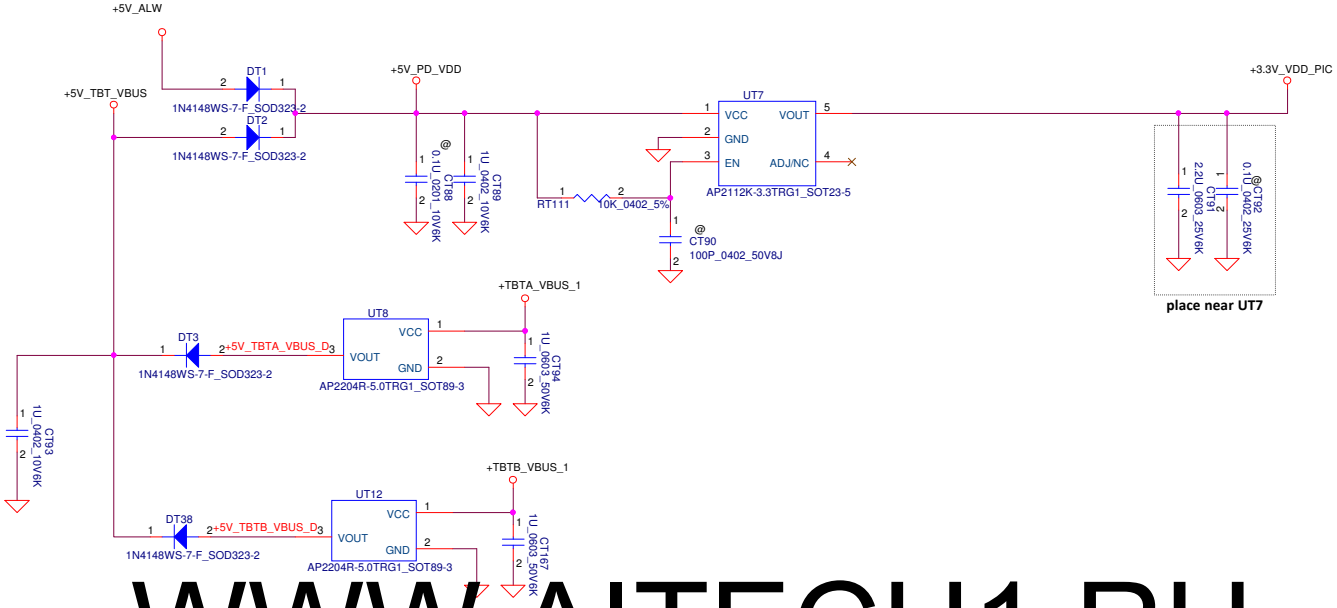
Compal Electronics, Inc.

Title: [Type C]PD Controller TI-2

Size | Document Number: LA-E112P | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 27 of 58

For kirkwood



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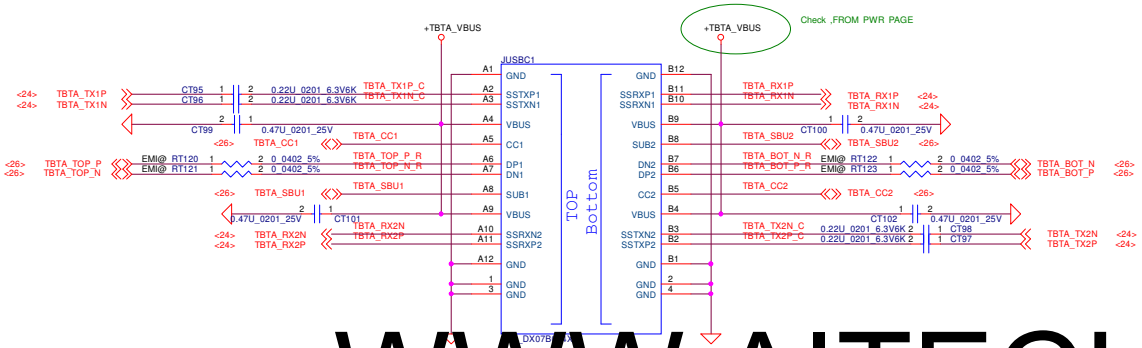
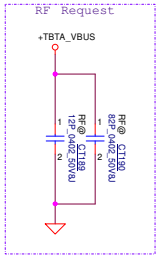
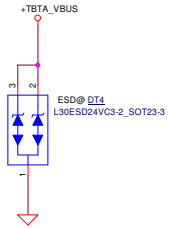
Compal Electronics, Inc.		
Title: [Type C]PD Power-2		
Size	Document Number: LA-E112P	Rev 0.1
Date: Friday, April 22, 2016	Sheet 28 of 58	

For AR Config







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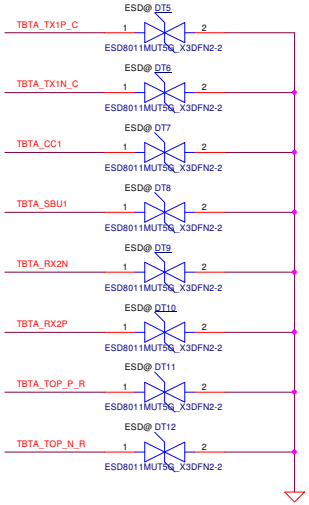

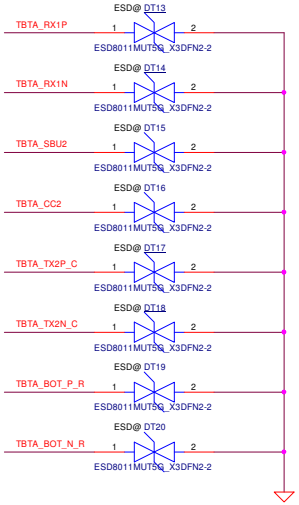

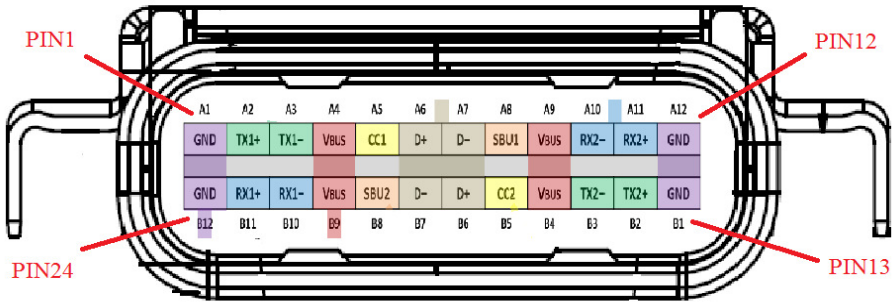

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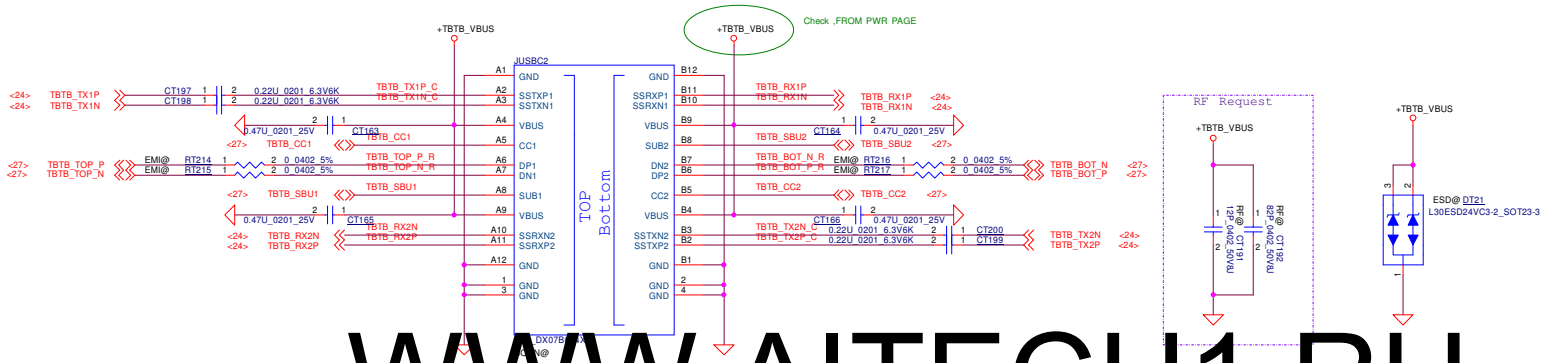
Compal Electronics, Inc.

Title: USB 3.0 CONN TYPE C

Size | Document Number: LA-E112P | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 29 of 58

For kirkwood



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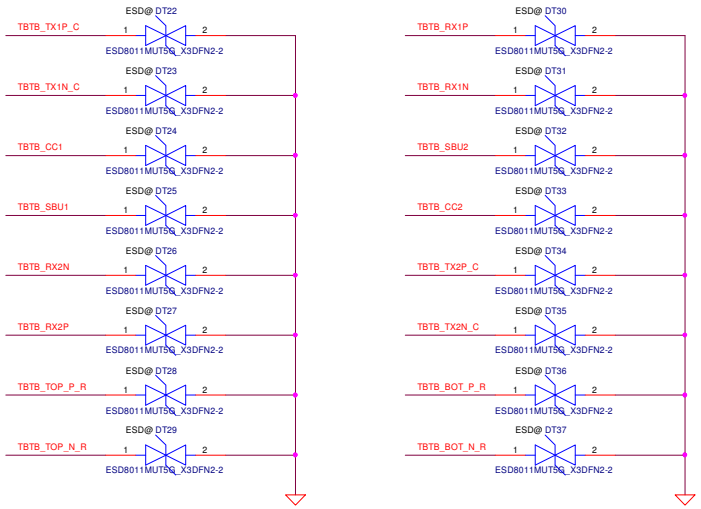

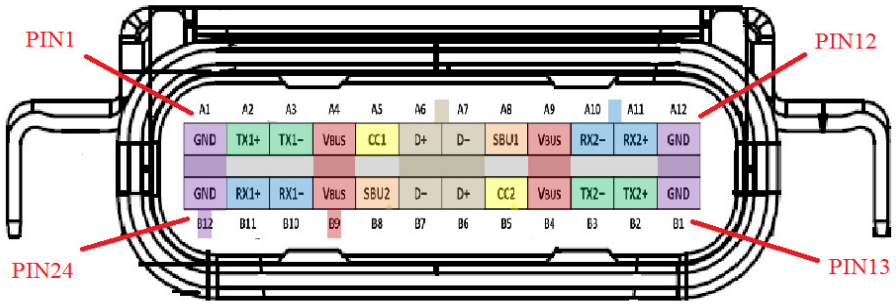

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Compal Electronics, Inc.

Title: USB 3.0 CONN TYPE C-2

Size | Document Number: LA-E112P | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 30 of 58

For Kirkwood

LINK 50398-04041-001 DONE
20160308

JEDP1
ACES_50398-04041-001
CONN@

DMIC0 <36>
DMIC_CLK0 <36>
+3.3V_RUN
+3.3V_CAM
USB20_N5_R
USB20_P5_R
CAM_MIC_CBL_DET# <12>
Pin15: LOOP_BACK
+BL_PWR_SRC
EMI@ LV11
DISP_ON
BIA_PWM
BLM15BB221SN1D_2P
EDP_HPD <6>
LCD_TST <37>
+LCDVDD
PANEL_SIZE_DET <12>
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EDP_AUXP_C
EDP_TXP0_C
EDP_TXN0_C
EDP_TXP1_C
EDP_TXN1_C
EDP_TXP2_C
EDP_TXN2_C
EDP_TXP3_C
EDP_TXN3_C
CV1 CV2 CV3 CV4 CV5 CV6 CV7 CV8 CV9 CV10
0.1U_0402_25V6
EDP_AUXN <6>
EDP_AUXP <6>
EDP_TXP0 <6>
EDP_TXN0 <6>
EDP_TXP1 <6>
EDP_TXN1 <6>
EDP_TXP2 <6>
EDP_TXN2 <6>
EDP_TXP3 <6>
EDP_TXN3 <6>
LCD_CBL_DET# <9>

@EMI@ CA5 100P_0402_50V8J
@EMI@ CA6 100P_0402_50V8J
EMI Request

EDP_HPD
@ RV7 100K_0402_5%
+LCDVDD
Reserve for EA

JTS2
ACES_50208-0060N-P01
CONN@
TS_SPI_IRQ <6>
TS_SPI_CS#_R <8>
TS_SPI_CLK_R <8>
TS_SPI_SI_R <8>
TS_SPI_SO_R <8>

Link ACES_50208-0060N-P01 done
20160315

+3.3V_TSP
TS_I2C_SDA
TS_I2C_SCL
RV98 2.2K_0402_5%
RV99 2.2K_0402_5%

JTS1
ACES_50208-01001-P03
CONN@
+3.3V_TSP
PCH_PLTRST#_AND <11,24,34,39,40>
TOUCH_SCREEN_PD# <12>
TS_I2C_SDA <9>
TS_I2C_SCL <9>
I2C0_IRQ_TS <6>
TOUCH_SCREEN_DET# <12>
RV305 10K_0402_5%
KKW

TOUCH_PANEL_PD#:
Close lid >> TP_EN = 0 >> Disable touch events
Open lid >> TP_EN = 1 >> Enable touch events
USB20_N8_R
USB20_P8_R
EXC24CQ900U_4P
LV27 EMI@
USB20_N8 <10>
USB20_P8 <10>

@ESD@ DV4 AZC199-02S3R7G_SOT23-3
ESD depop locat i on

LINK ACES_50208-01001-P03 Done
20160321

TS_SPI_CS#_R
TS_SPI_CLK_R
TS_SPI_SI_R
TS_SPI_SO_R
TS_I2C_SDA
TS_I2C_SCL
RF@CV50 33P_0402_50V8J
RF@CV51 33P_0402_50V8J
RF@CV52 33P_0402_50V8J
RF@CV53 33P_0402_50V8J
RF@CV54 33P_0402_50V8J
RF@CV55 33P_0402_50V8J
RF Request

+BL_PWR_SRC
+LCDVDD
+3.3V_CAM
+3.3V_TSP
+3.3V_RUN
0.1U_0603_50V7K @CV11
0.1U_0201_10V6K @CV12
0.1U_0201_10V6K @CZ1
0.1U_0201_10V6K @CZ2
0.1U_0201_10V6K @CZ4
Close to JEDP1.17~19
Close to JEDP1.30~31
Close to JEDP1.11
Close to JEDP1.1
Close to JEDP1.10

RF Request
+3.3V_TSP
RF@ CV18 82P_0402_50V8J
RF@ CV19 12P_0402_50V8J

JIR1
ACES_50208-0060N-P01
CONN@
IR_CAM_DET# <12>
+PWR_SRC

Link ACES_50208-0060N-P01 done
20160315

+PWR_SRC
RF@ CZ3 100P_0402_50V8J
RF Request

+3.3V_RUN
RV8 10K_0402_5%
TOUCH_SCREEN_DET#

DV1 BAT54CW_SOT323-3
BIA_PWM
EDP_BIA_PWM <6>
BIA_PWM_EC <37>
RV1 47K_0402_5%

DV2 BAT54CW_SOT323-3
DISP_ON
PANEL_BKLEN <6>
PANEL_BKEN_EC <37>

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RF Request
+LCDVDD
+3.3V_CAM
+BL_PWR_SRC
RF@ CV20 12P_0402_50V8J
RF@ CV21 82P_0402_50V8J
RF@ CV22 12P_0402_50V8J
RF@ CV23 82P_0402_50V8J
RF@ CV24 12P_0402_50V8J
RF@ CV25 82P_0402_50V8J

CHECK Power Rail
+3.3V_RUN
+3.3V_TSP
+3.3V_RUN
RV9 10K_0402_5%
QV8 LP2301ALT1G_SOT23-3
<9> 3.3V_TS_EN
RV306 0_0402_5%
QV7 L2N7002WT1G_SC-70-3

WebCAM

+3.3V_CAM
+3.3V_RUN
QZ1 LP2301ALT1G_SOT23-3
<11> 3.3V_CAM_EN#
<10> USB20_P5
<10> USB20_N5
EXC24CQ900U_4P
LZ1 EMI@
USB20_P5_R
USB20_N5_R

Backlight POWER

+PWR_SRC
+BL_PWR_SRC
QV1 AO6405_TSOP6
CV13 1000P_0402_50V7K
RV4 270K_0402_5%
CV15 0.1U_0603_50V7K
BL_PWR_SRC_ON
QV2 L2N7002WT1G_SC-70-3
RV5 47K_0402_5%
CV14 0.01U_0402_50V7K
<37> EN_INVPWR

LCDVDD POWER

+LCDVDD
+EDP_VDD
+3.3V_ALW
@CV16 10U_0603_10V6M
PJP12 PAD-OPEN1x1m
UV24 G524B1T11U_SOT23-5
VOUT
GND
/OC
VIN
EN
@CV17 0.01UF_0402_25V7K
DV3 BAT54CW_SOT323-3
<37> LCD_VCC_TEST_EN
<6,37> ENVDD_PCH
EN_LCDPWR
RV3 100K_0402_5%

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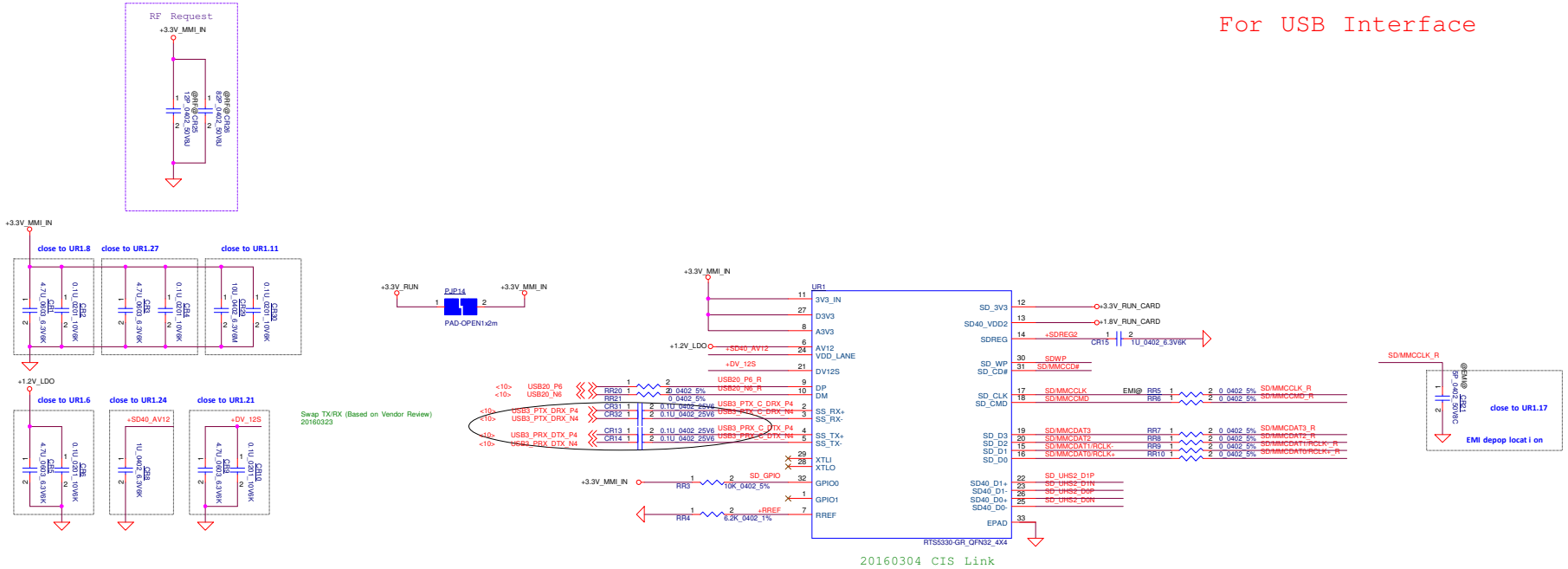
Compal Electronics, Inc.

Title: eDP CONN & Touch screen

Size | Document Number: LA-E112P | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 31 of 58

For USB Interface



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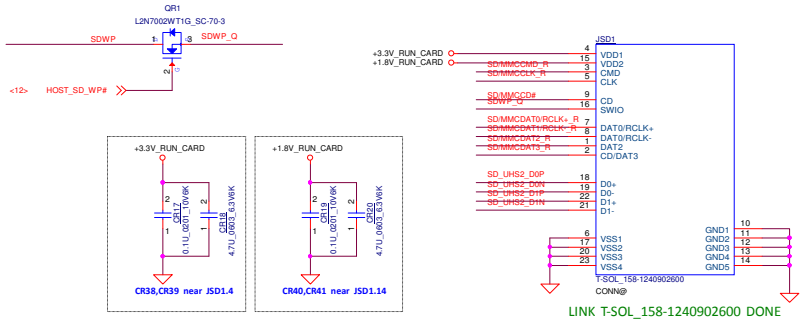
HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
	Low	High	Write Protect(FW LOCK)



LINK T-SOL_158-1240902600 DONE 20160329

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Compal Electronics, Inc.

Title: Card Reader RTS5330

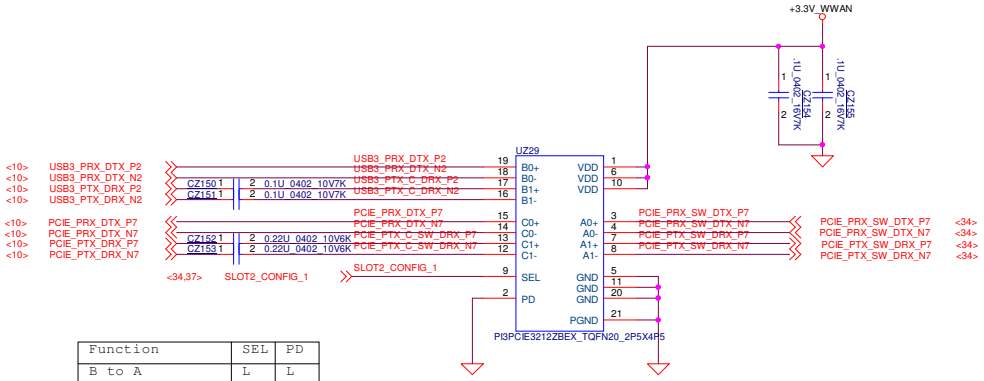
Size: | Document Number: LA-E112P | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 32 of 58

Only for Kirkwood

PCIE/USB MUX

NEED LINK TI HD3SS3212 as main



Function	SEL	PD
B to A	L	L
C to A	H	L
All ports Hi-Z, IC power down	X	H

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STATE	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD-PCIE(4 lane)
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)
8	HIGH	GND	GND	GND	WWAN
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)
15	HIGH	HIGH	HIGH	HIGH	NA

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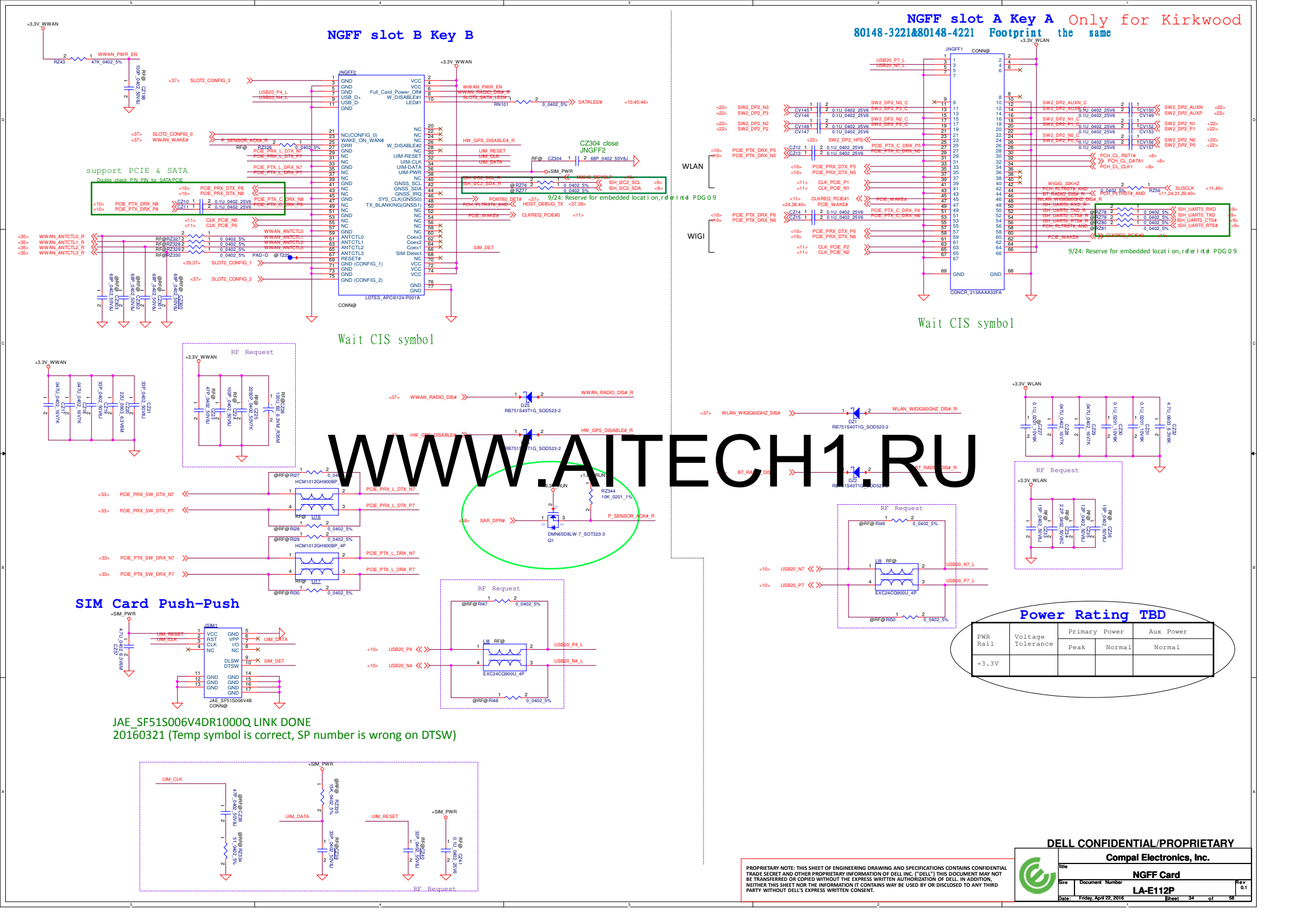
Compal Electronics, Inc.

Title: USB/PCIE MUX

Size | Document Number: LA-E112P | Rev 0.1

Date: Friday, April 22, 2016 | Sheet 33 of 58



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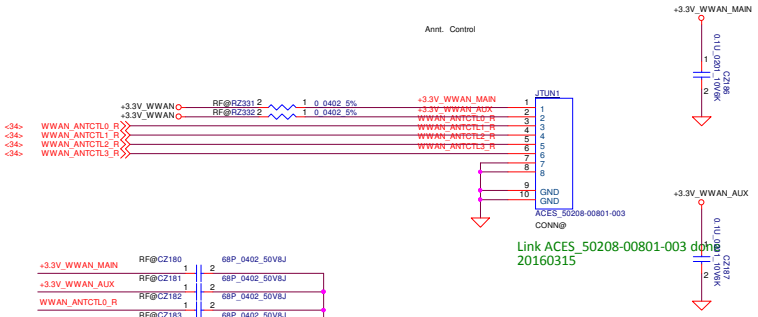
Only for Kirkwood



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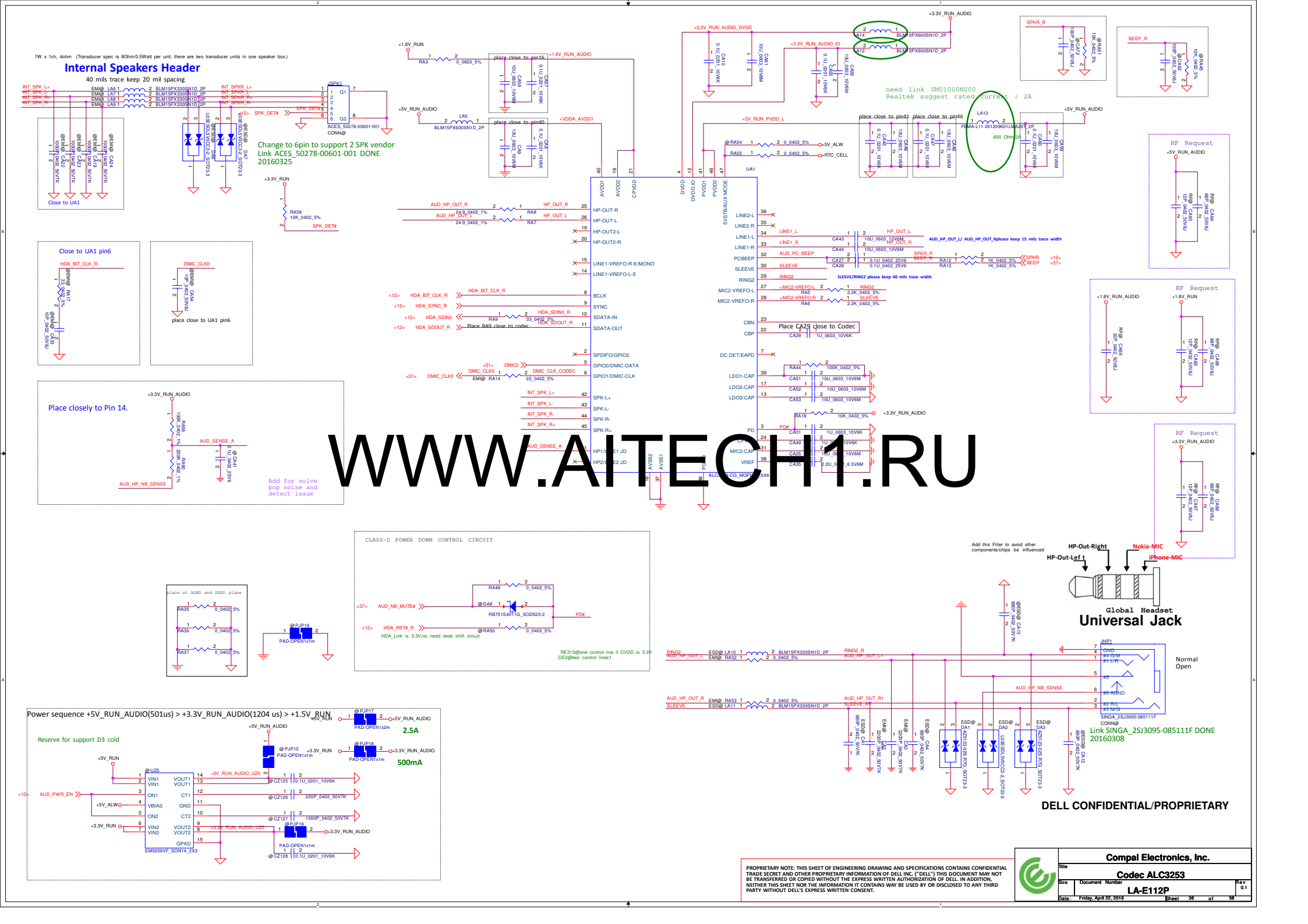
Compal Electronics, Inc.

Title: RF Tunable Conn

Size | Document Number: LA-E112P | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 35 of 58



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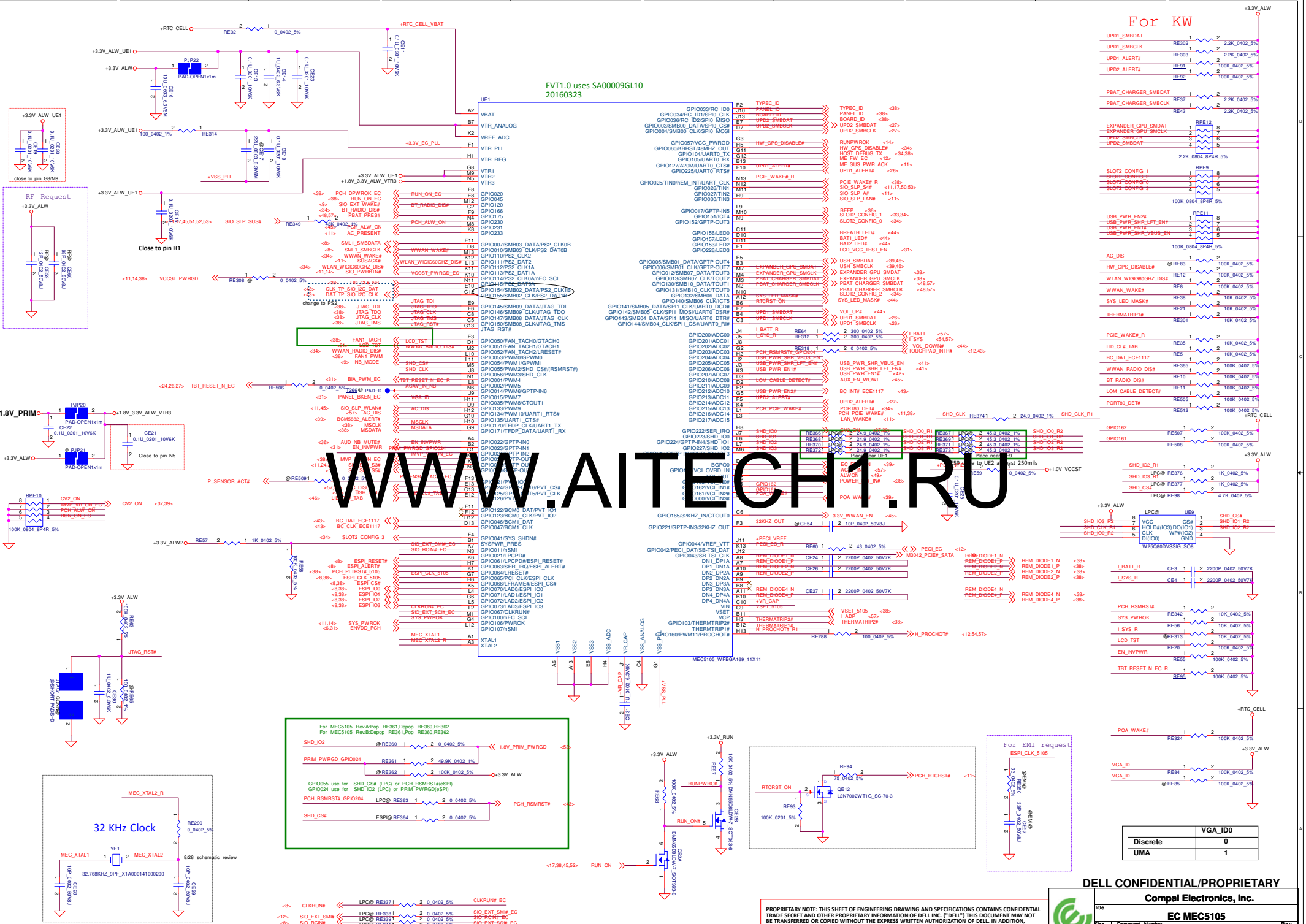

	VGA_ID0
Discrete	0
UMA	1

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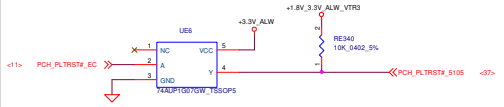
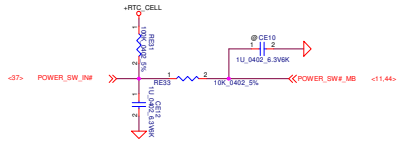
Compal Electronics, Inc.

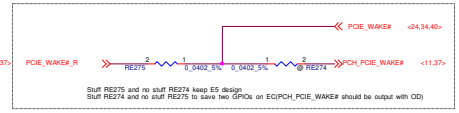
Title: EC MEC5105

Size: | Document Number: LA-E112P | Rev: 0.1

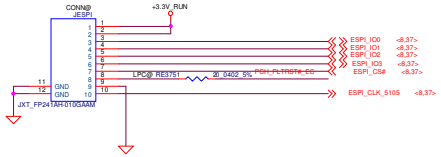
Date: Friday, April 22, 2016 | Sheet 37 of 58

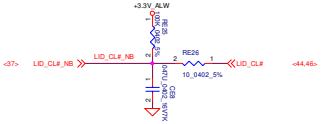


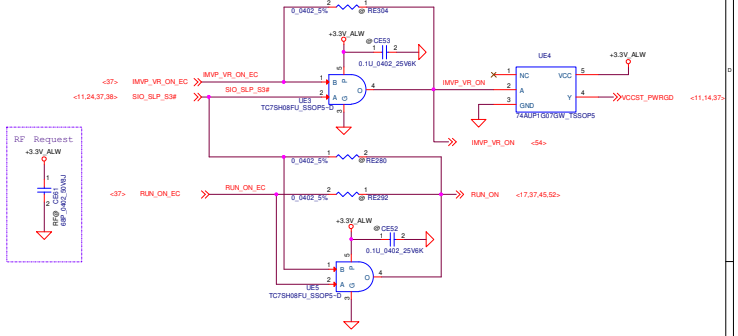


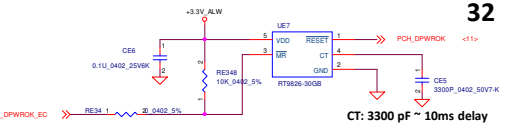


PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	

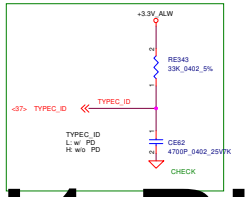




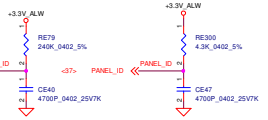




Reset Threshold Level 3.0V



RE343	CE62	REV
240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/ AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	
2K	4700p	
1K	4700p	



RE79	CE40	REV
* 240K	4700p	X00
130K	4700p	
62K	4700p	
33K	4700p	
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

RE300	CE47	PANEL SIZE
240K	4700p	SB/BR 12"
130K	4700p	SB/BR 14"
33K	4700p	BR 15"
* 4.3K	4700p	KW 12/13"

BOARD_ID rise time is measured from 5%~68%

PANEL_ID rise time is measured from 5%~68%

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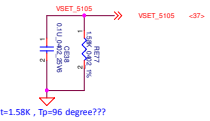
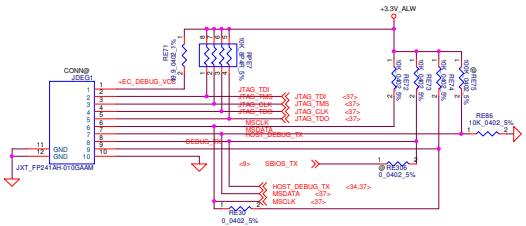
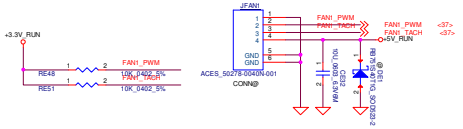


Rest=1.58K , Tp=96 degree???



Link ACES_50278-0040N-001 DONE
20160331

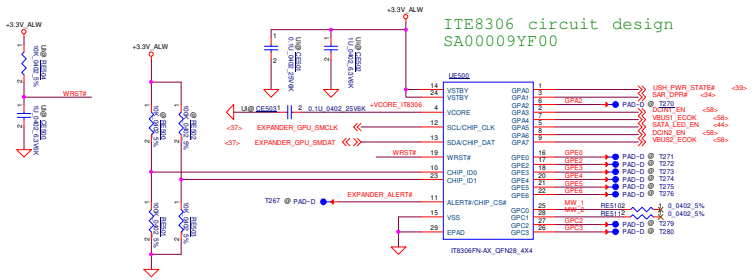


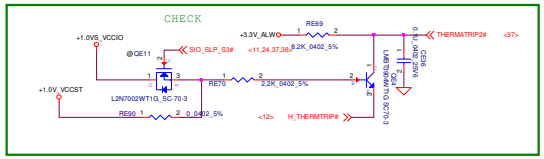
Control Byte

0	1	0	0	0	A1	A0	R/W

R/W = 0 = Wirte
R/W = 1 = Read

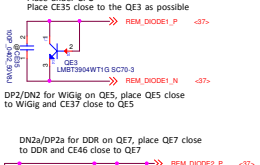
SMBus address 0x40

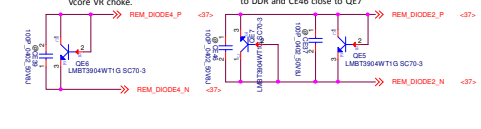




Thermal diode mapping

5085 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)





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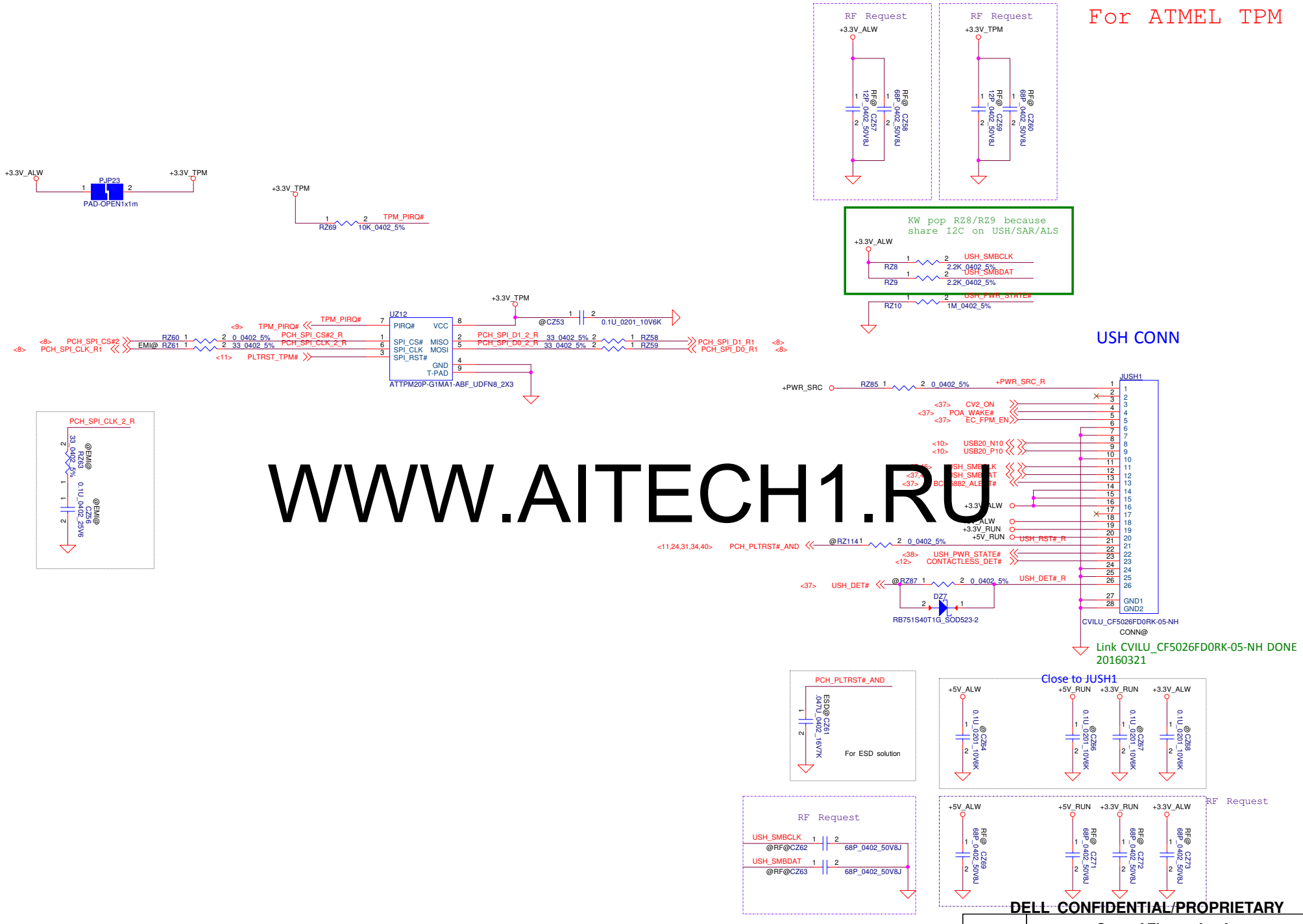
Title	MEC5085	
Size / Document Number	LA-E112P	Rev 0.1
Date: Friday, April 22, 2016	Sheet 38 of 58	

For ATMEL TPM



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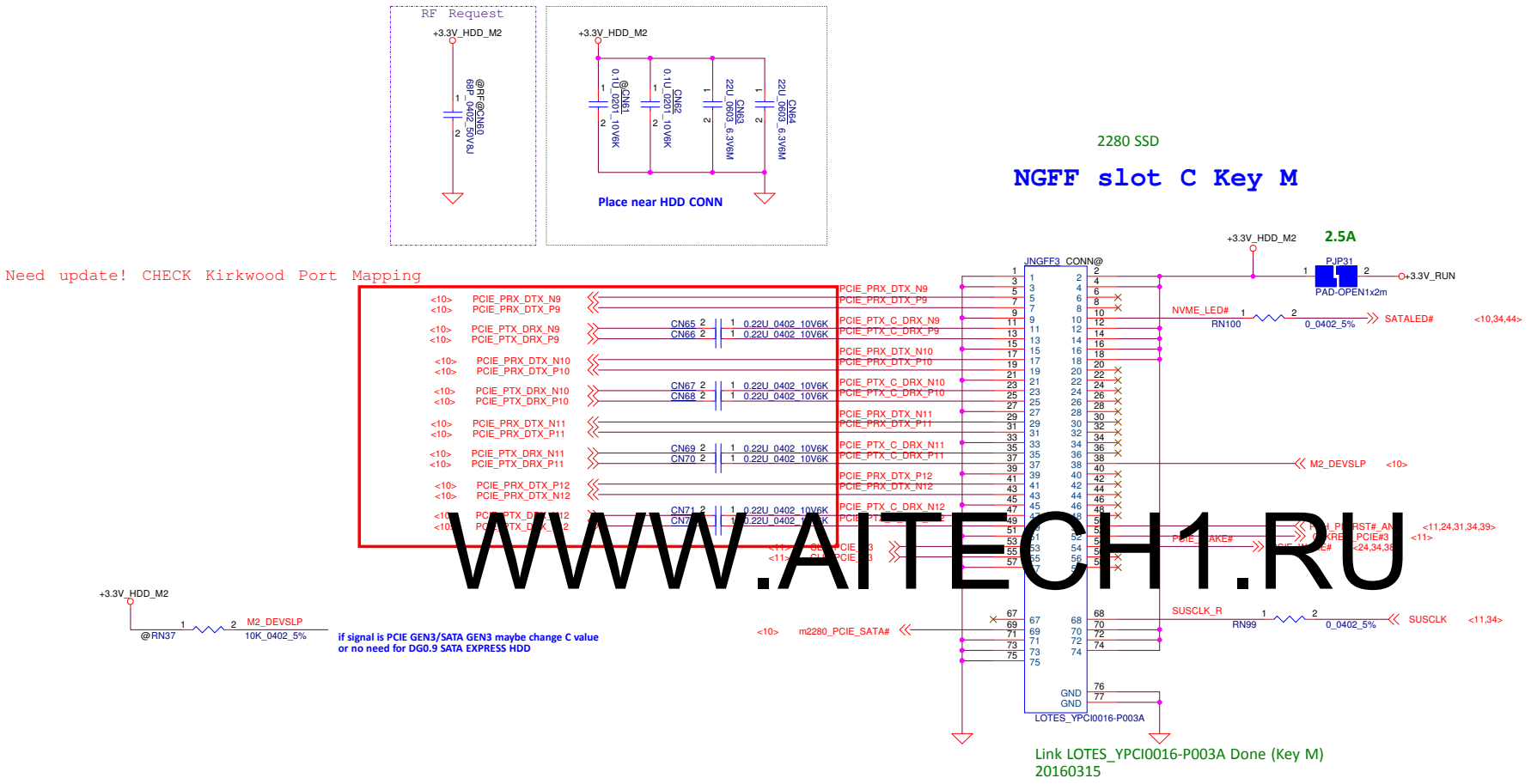
Compal Electronics, Inc.
Title: USH & TPM
Size | Document Number: LA-E112P | Rev 0.1
Date: Friday, April 22, 2016 | Sheet 39 of 58

For PCIEX4,Kirkwood



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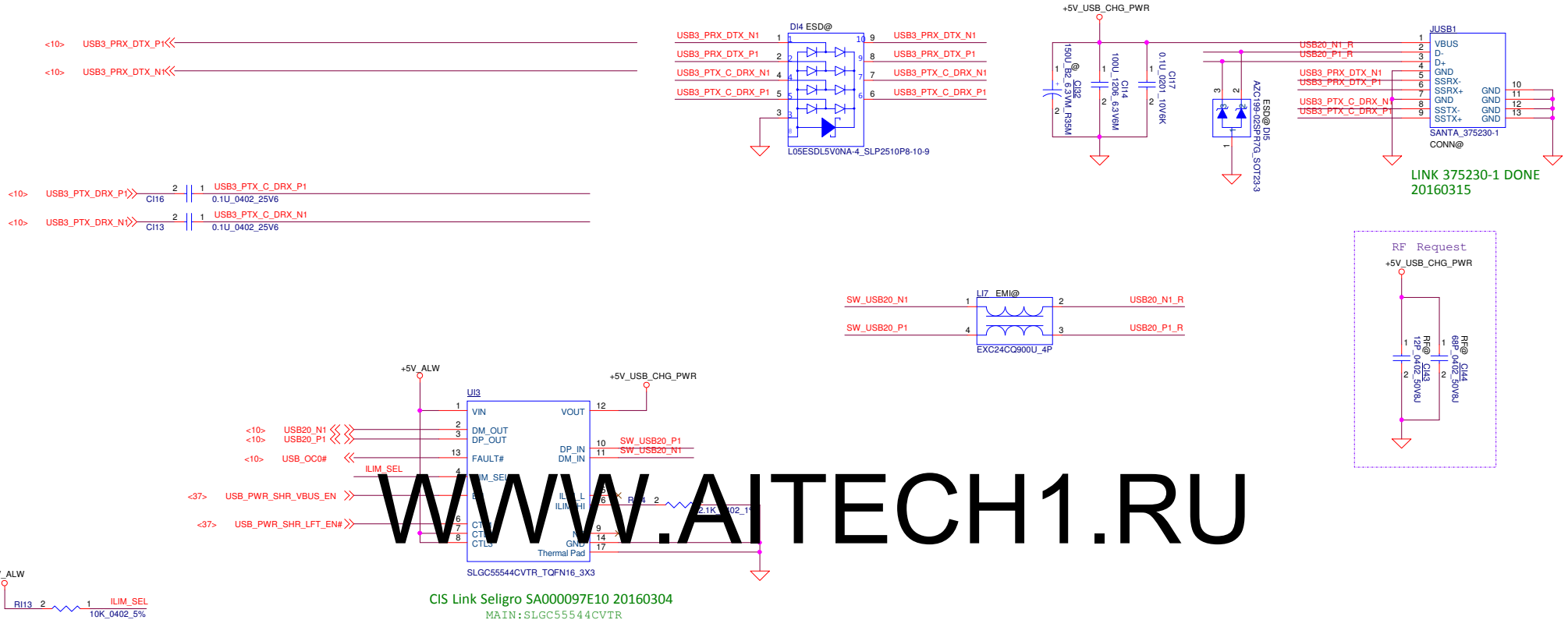
Compal Electronics, Inc.

Title: M2 2280 Socket

Size | Document Number: LA-E112P | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 40 of 58

For PWR SW + Charger combine IC



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Compal Electronics, Inc.

Title	JUSB1+PS
Size	
Document Number	LA-E112P
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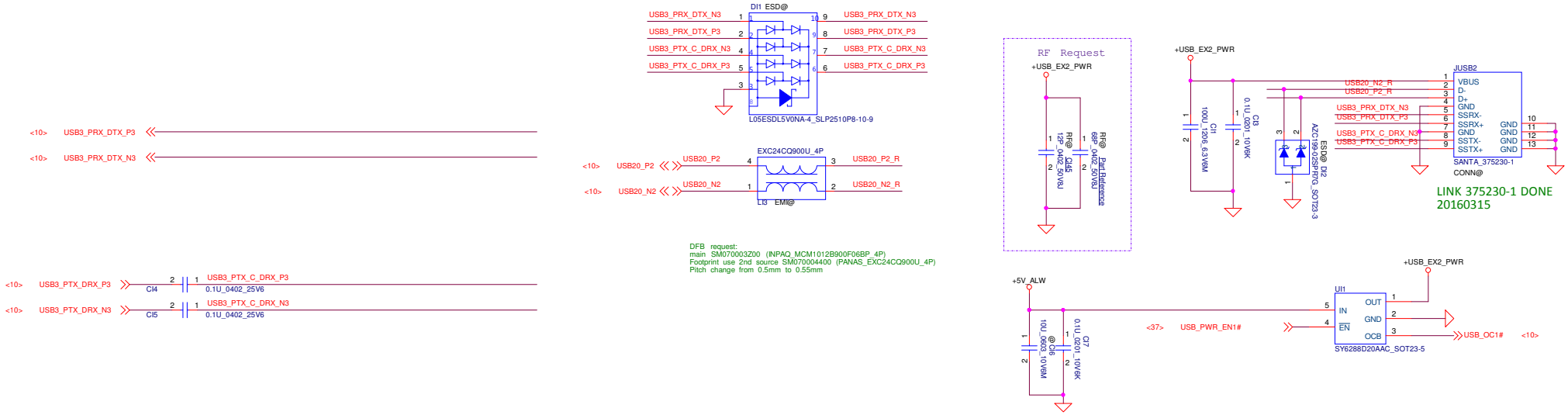
For Breckenridge/Steamboat 12&Kirkwood



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Compal Electronics, Inc.			
Title: JUSB2			
Size	Document Number: LA-E112P		Rev 0.1
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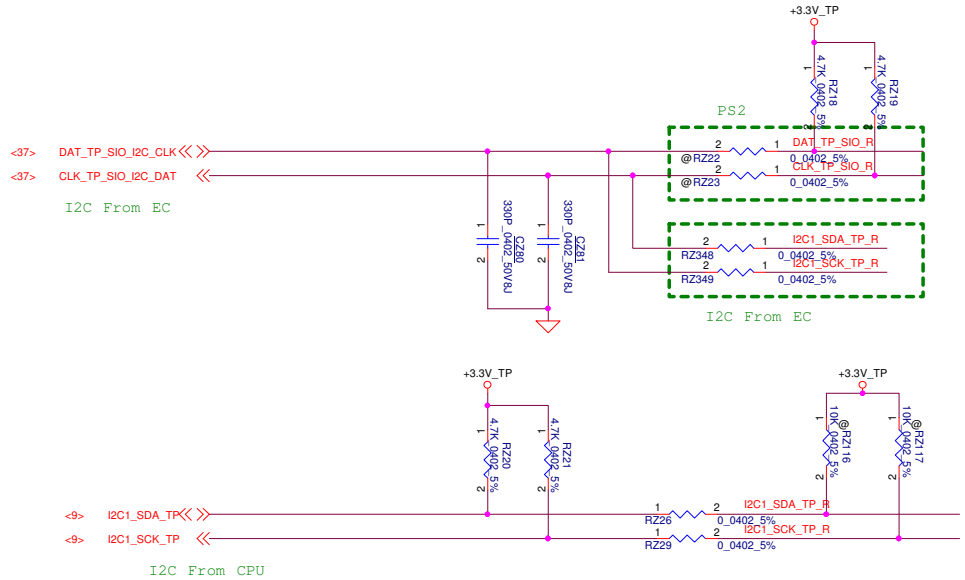
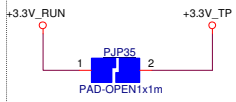
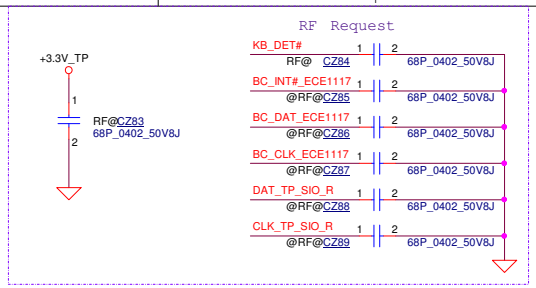
Touch Pad

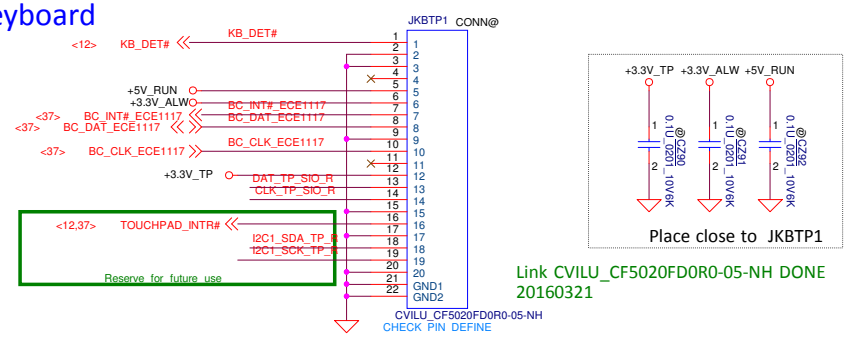


Plan is for I2C to be driven by the EC for Win7 and the PCH (with utility Intel I2C driver for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will have I2C driven in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues





Keyboard



Link CVILU_CF5020FD0R0-05-NH DONE 20160321

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@eDP Cable W CAM

Part Number	Description
DC02C007600	H-CONN SET 13D MB-EDP-CAMERA

@eDP TS Cable W CAM

Part Number	Description
DC02C007C00	H-CONN SET 13D MB-EDP-CAMERA-TS

@eDP Cable W/O CAM

Part Number	Description
DC02C007D00	H-CONN SET 13D MB-EDP

@SATA SPINDLE Cable

Part Number	Description
DC02C007500	H-CONN SET 13D MB-SPINDLE HDD

@SATA Cable

Part Number	Description
DC02C007400	H-CONN SET 13D MB-MSATA HDD

@DC-IN Cable

Part Number	Description
DC30100Q100	CONN SET 13F DCJACK-MB 2DW1003-041110F

@BATT Cable

Part Number	Description
DC02001X800	H-CONN SET 13D MB-BATT CABLE

@LED FFC

Part Number	Description
NBX0001JG00	FFC 10P F P0.5 PAD0.3 172MM MB-LED/B 13D

@FP FFC

Part Number	Description
NBX0001JK00	FFC 8P F P0.5 PAD.3 123MM MB-FP VALIDITY

@TP FFC

Part Number	Description
NBX0001JI00	FFC 16P F P0.5 PAD=0.3 119MM MB-TP 13D

@USH Board FFC

Part Number	Description
NBX0001JJ00	FFC 26P G P0.5 PAD.3 88MM MB-USH/B 13D

@RTC BATT

Part Number	Description
GC02001DS00	BATT CR2032 3V 225MAH PA 5 W/C 30MM

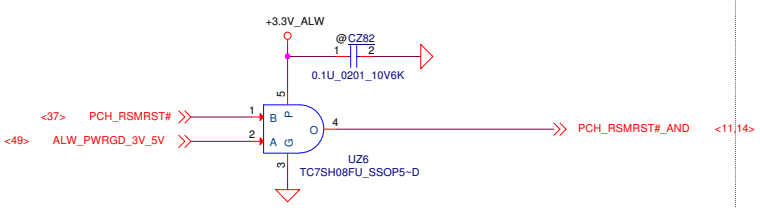
@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@Speak

Part Number	Description
PK230003Q0L	SPK PACK 2JX 2.0W 4 OHM FG

RSMRST circuit



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Compal Electronics, Inc.

Title: Keyboard

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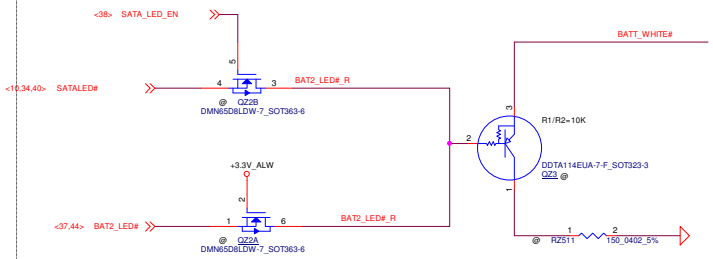
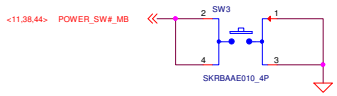
HDD LED MUX

means EC can switch battery white led and HDD LED by hot key " Fn+H



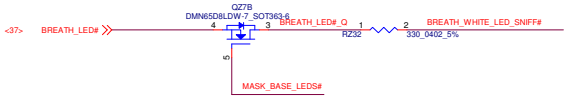
Battery LED

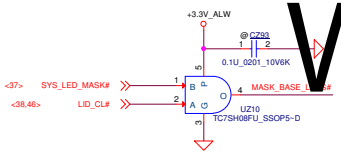
POWER & INSTANT ON SWITCH For NPI USE



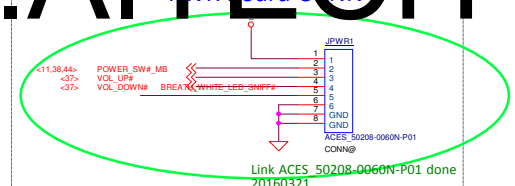
Breath LED

LED P/N change to SC50000FL00 from SC50000BA00



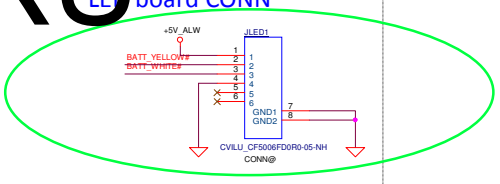


PWR board CONN



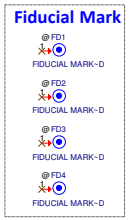
Link ACES_50208-0060N-P01 done 20160321

LED board CONN



Link CVILU_CF5006FD0R0-05-NH done 20160325

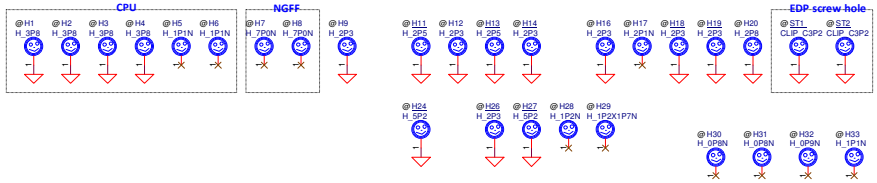
Fiducial Mark

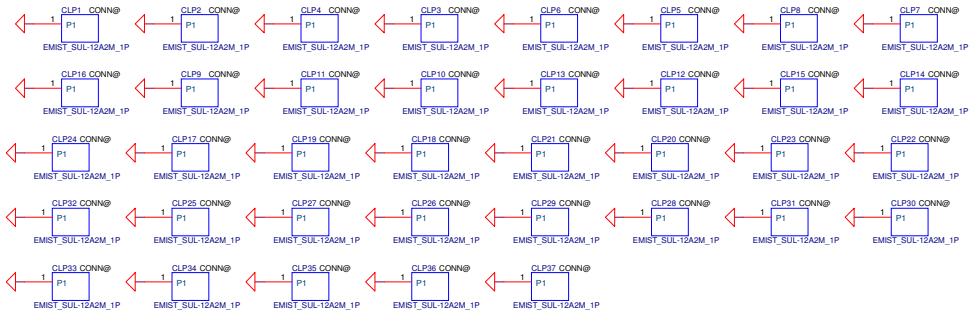


LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

For JAE JSIM1 boss hole





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Compal Electronics, Inc.

Title: PAD, LED

Size: | Document Number: LA-E112P | Rev: 0.1

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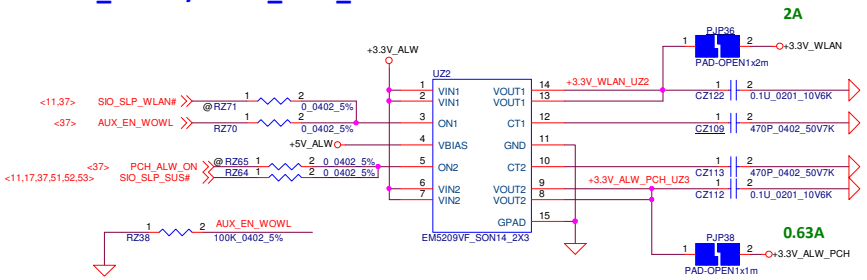
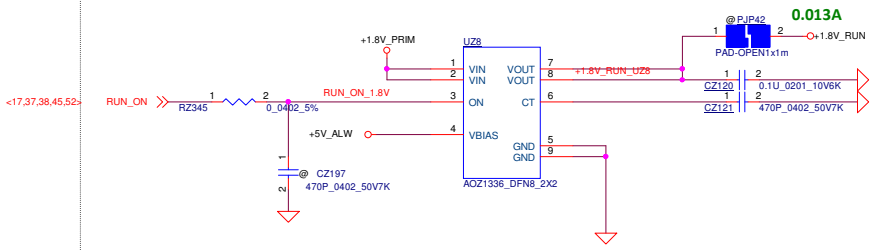
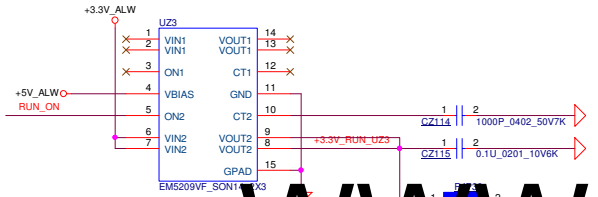
+3.3V_WLAN/+3.3V_ALW_PCH source



+1.8V_RUN source



+3.3V_RUN source



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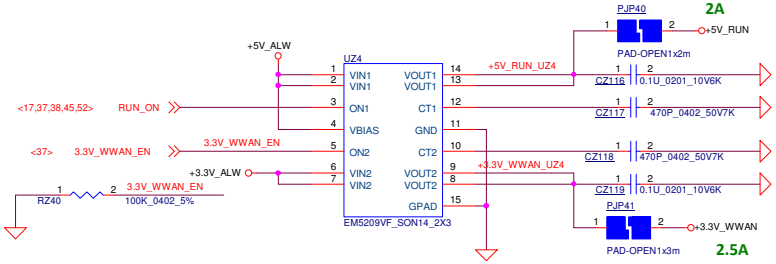
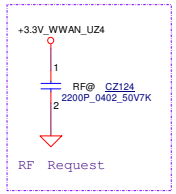
+5V_RUN/+3.3V_WWAN source





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DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: Power control

Size | Document Number: LA-E112P | Rev: 0.1

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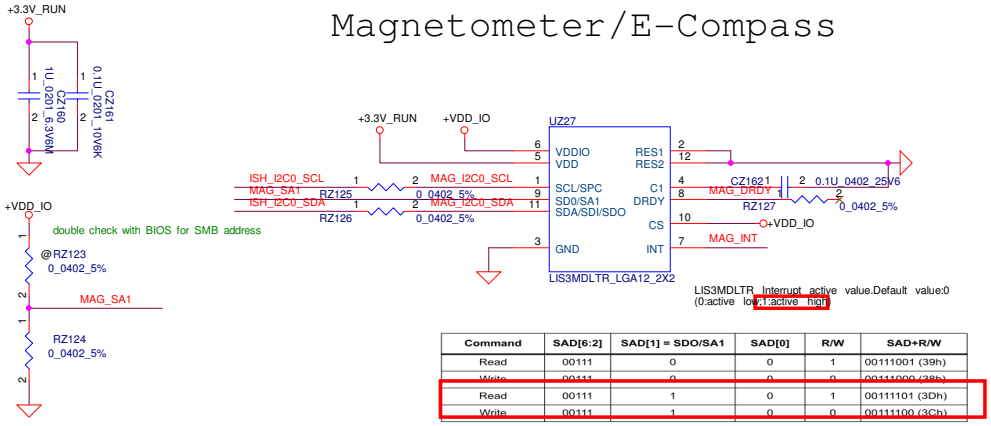
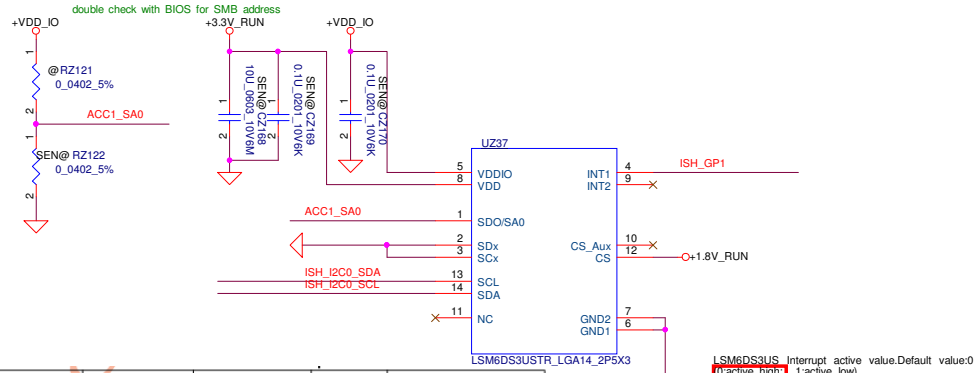
Only for Kirkwood

Magnetometer/E-Compass



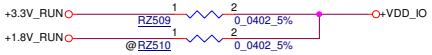
Command	SAD[6:2]	SAD[1] = SDO/SA1	SAD[0]	R/W	SAD+R/W
Read	00111	0	0	1	00111001 (39h)
Write	00111	0	0	0	00111000 (38h)
Read	00111	1	0	1	00111101 (3Dh)
Write	00111	1	0	0	00111100 (3Ch)

3D accelerometer and Gyro sensor

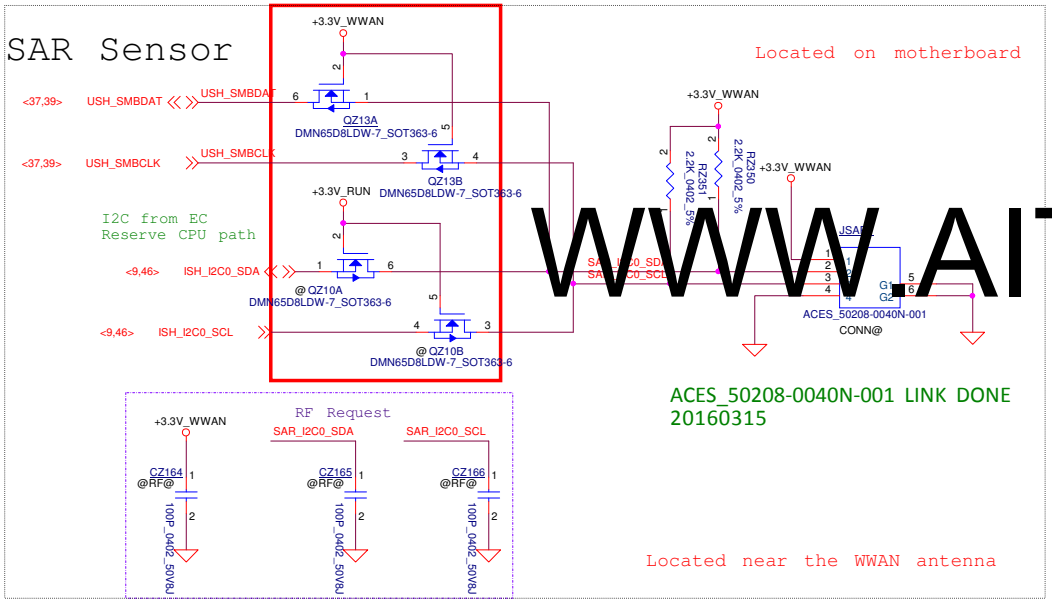


Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	110101	0	1	11010101 (D5h)
Write	110101	0	0	11010100 (D4h)
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

Located on MB



SAR Sensor

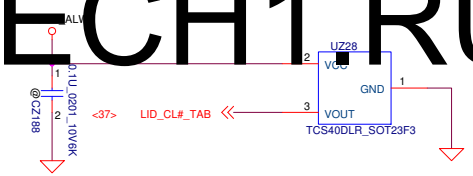


Located on motherboard

ACES_50208-0040N-001 LINK DONE
20160315

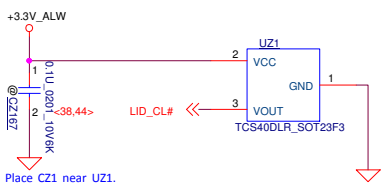
Located near the WWAN antenna

Detect closed in tablet position



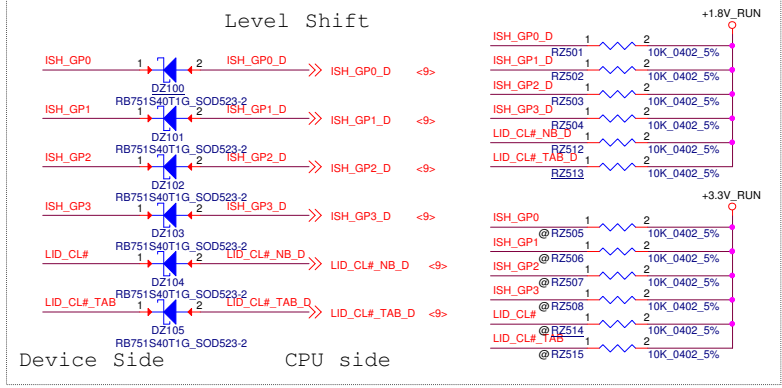
Hall sensor: SA00009CB00

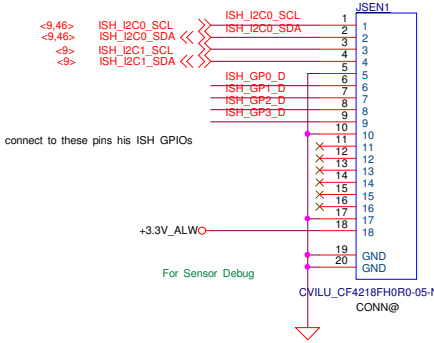
Detect clamshell closed

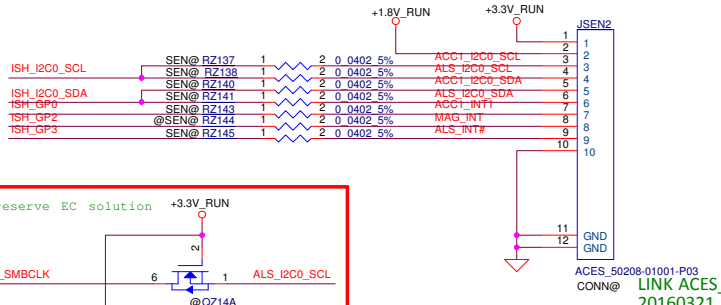


Hall sensor: SA00009CB00

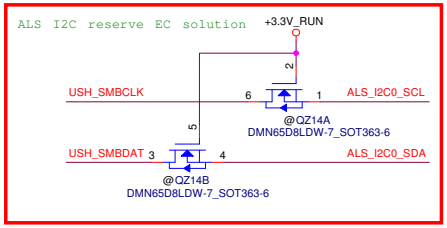
Level Shift







LINK ACES_50208-01001-P03 Done
20160321



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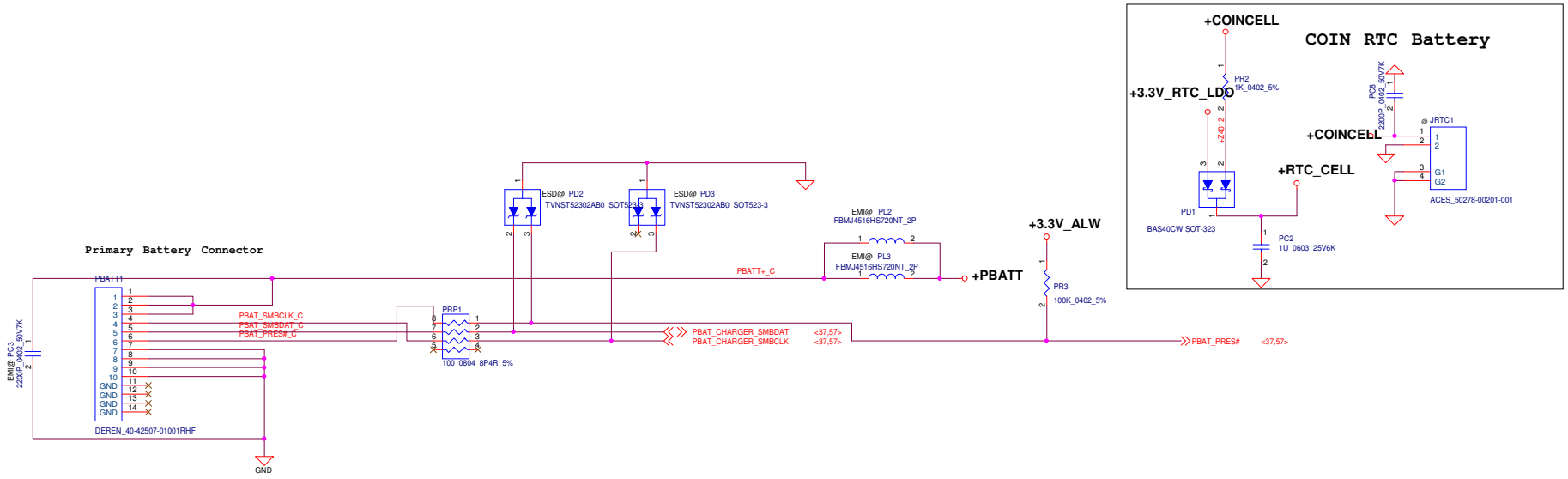
Title: SENSOR

Size | Document Number: LA-E112P | Rev 0.1

Date: Friday, April 22, 2016 | Sheet 46 of 58



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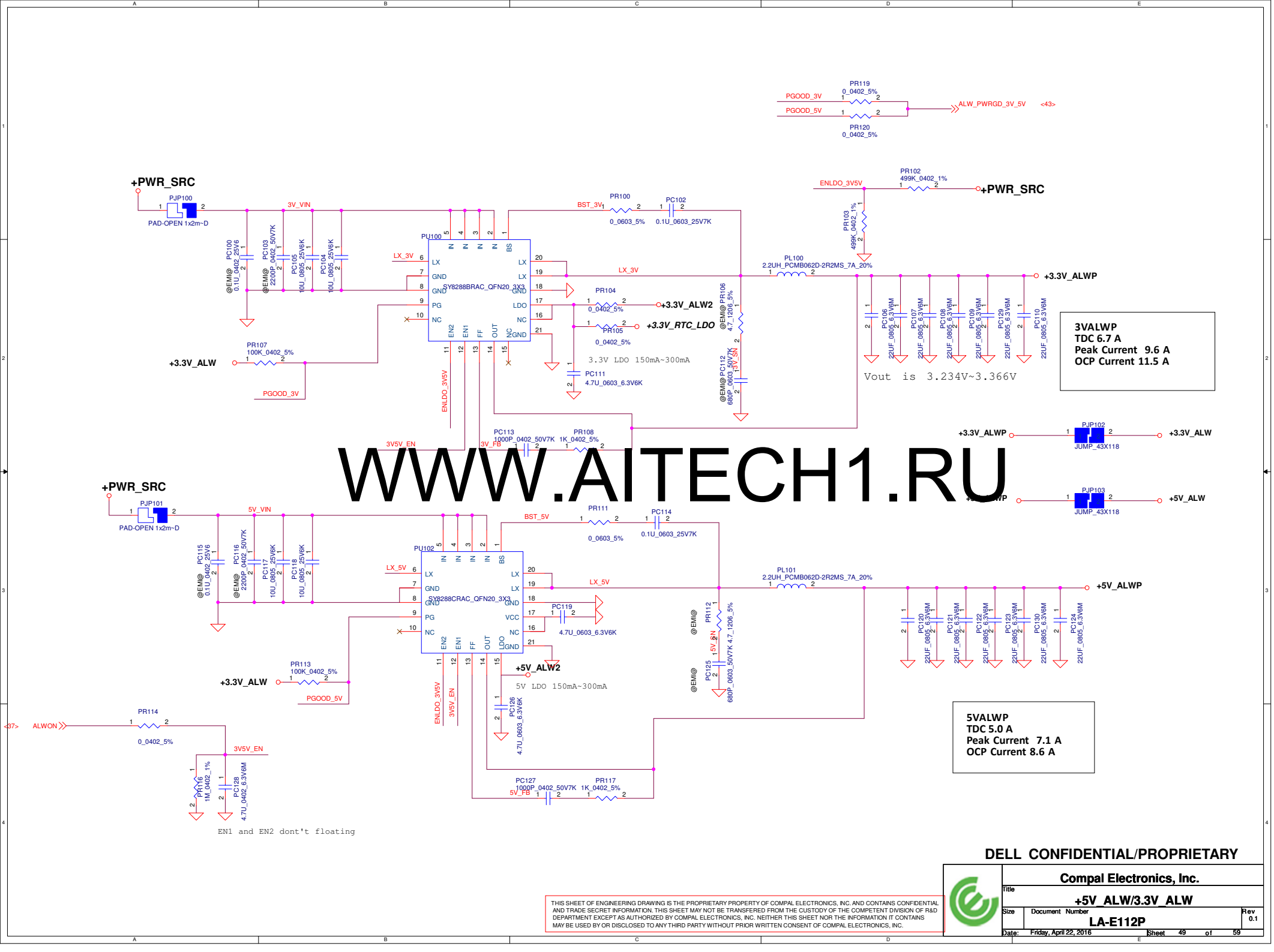
Compal Electronics, Inc.		
Title: +DCIN		
Size	Document Number: LA-E112P	Rev 0.1
Date: Friday, April 22, 2016	Sheet 48 of 59	



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Compal Electronics, Inc.

Title: +5V_ALW/3.3V_ALW

Size | Document Number: LA-E112P | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 49 of 59

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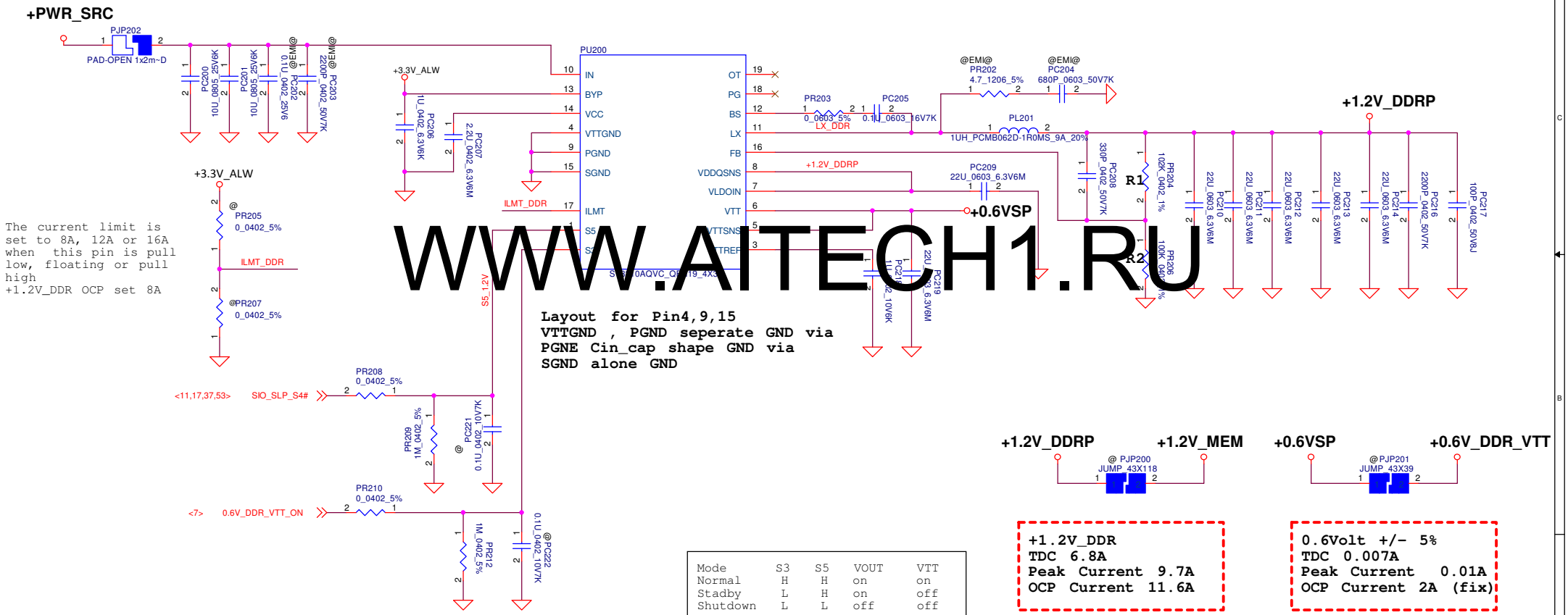

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Mode	S3	S5	VOUT	VTT
Normal	H	H	on	on
Stadby	L	H	on	off
Shutdown	L	L	off	off

Note: S3 - sleep ; S5 - power off

+1.2V_DDR
TDC 6.8A
Peak Current 9.7A
OCP Current 11.6A

0.6Volt +/- 5%
TDC 0.007A
Peak Current 0.01A
OCP Current 2A (fix)

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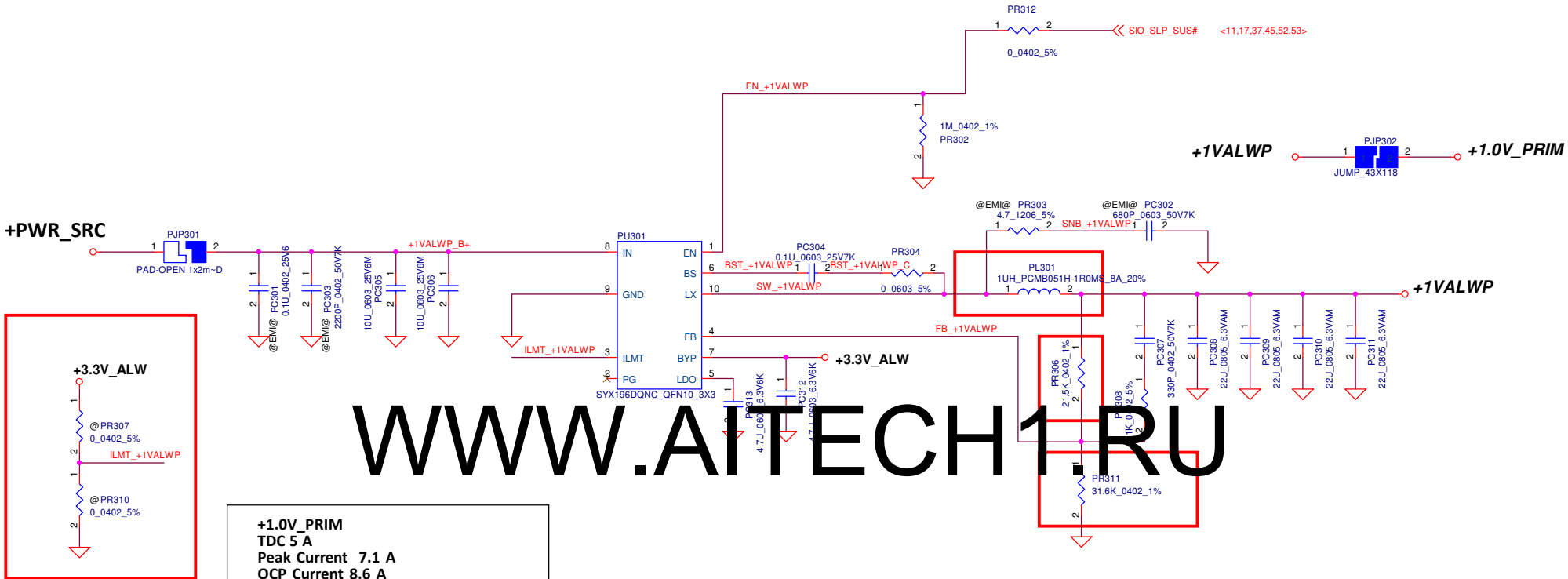
Compal Electronics, Inc.

Title: +1.2V_MEN/+0.6V_DDR_VTT

Size | Document Number: LA-E112P | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 50 of 59



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+1.0V_PRIM
TDC 5 A
Peak Current 7.1 A
OCP Current 8.6 A

	TYP	MAX
Choke DCR	15.0mohm ,	17.0mohm

The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

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Title	**+1VALWP**	
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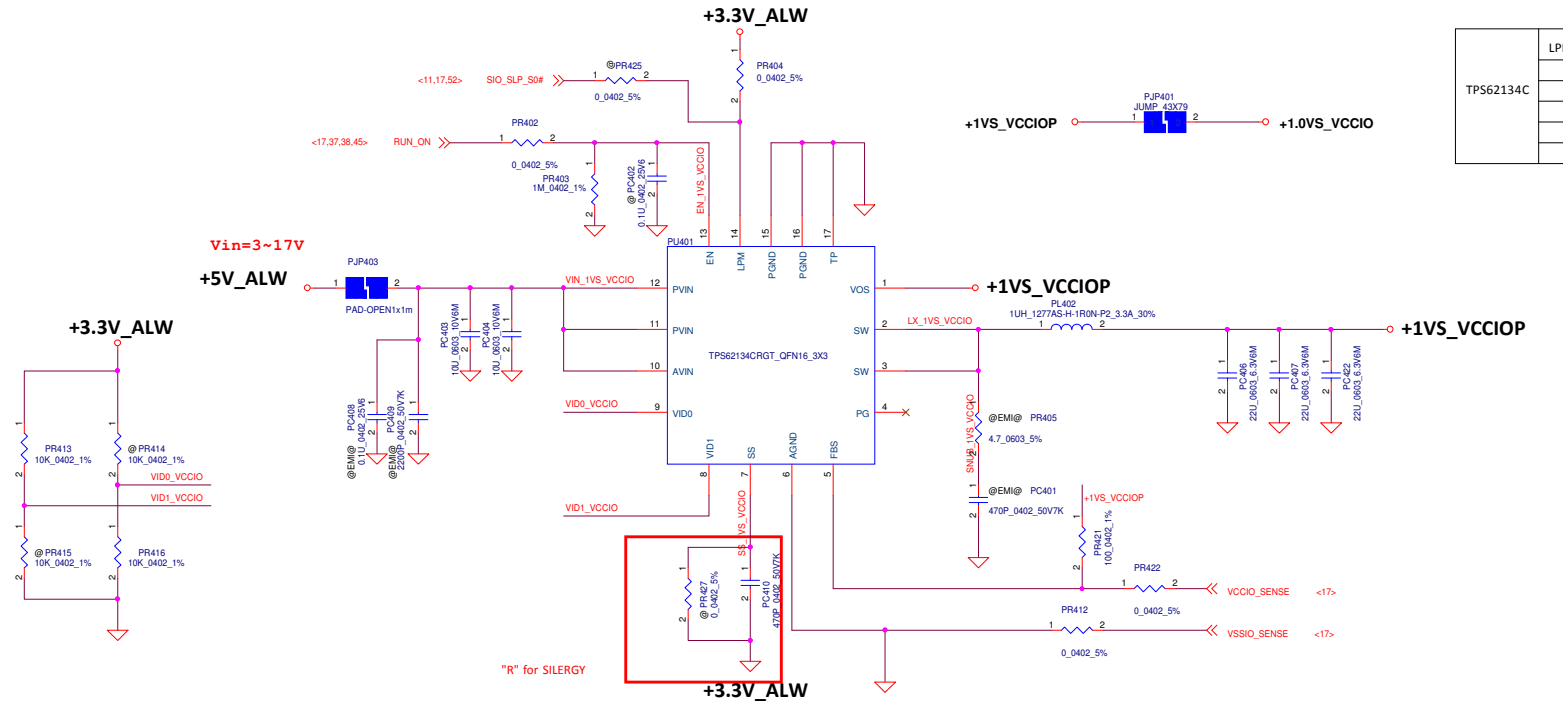

	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
TPS62134C	0	X	X	0(LPM)
	1	0	0	0.80
	1	0	1	0.95
	1	1	0	1.00
	1	1	1	1.05

+1.0VS_VCCIO
TDC 1.9 A
Peak Current 2.7 A
OCP Current 3.3 A
TYP MAX
Choke DCR 48.0mohm

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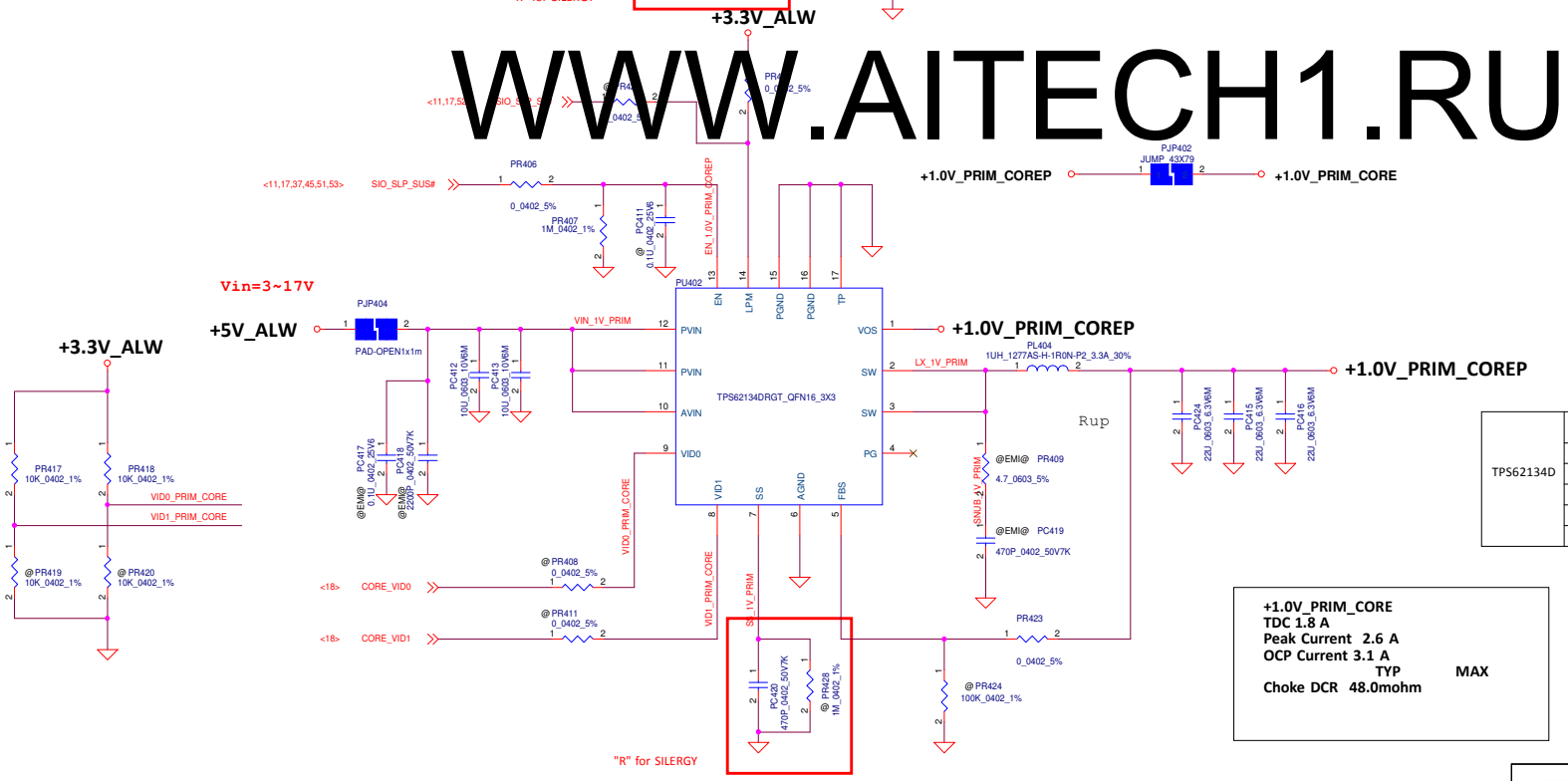

	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
TPS62134D	0	X	X	0.7(LPM)
	1	0	0	0.85
	1	0	1	0.90
	1	1	0	0.95
	1	1	1	1.00

+1.0V_PRIM_CORE
TDC 1.8 A
Peak Current 2.6 A
OCP Current 3.1 A
TYP MAX
Choke DCR 48.0mohm

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Title: **+1VS_VCCIOP/+1.0V_PRIM_COREP**

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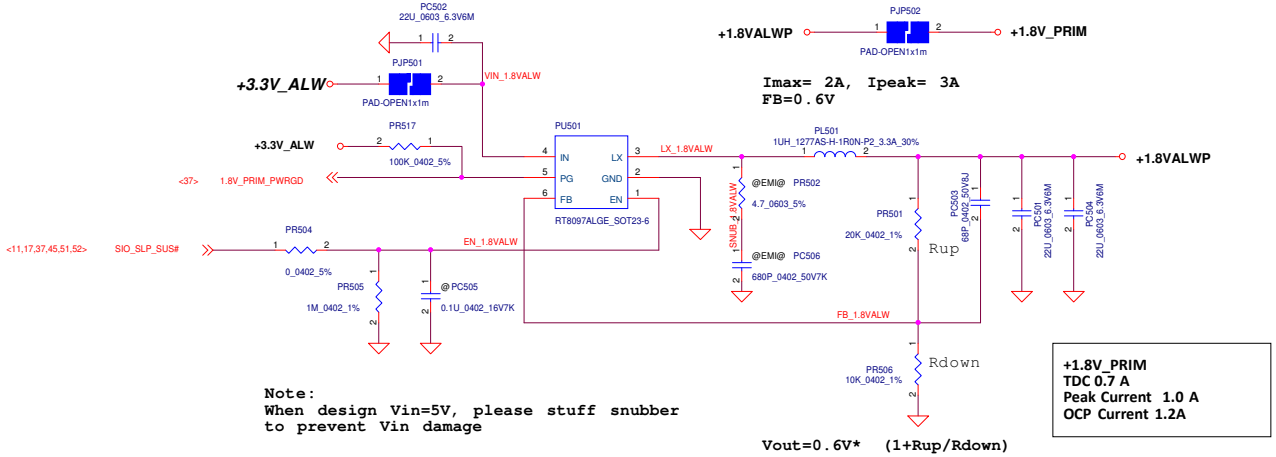

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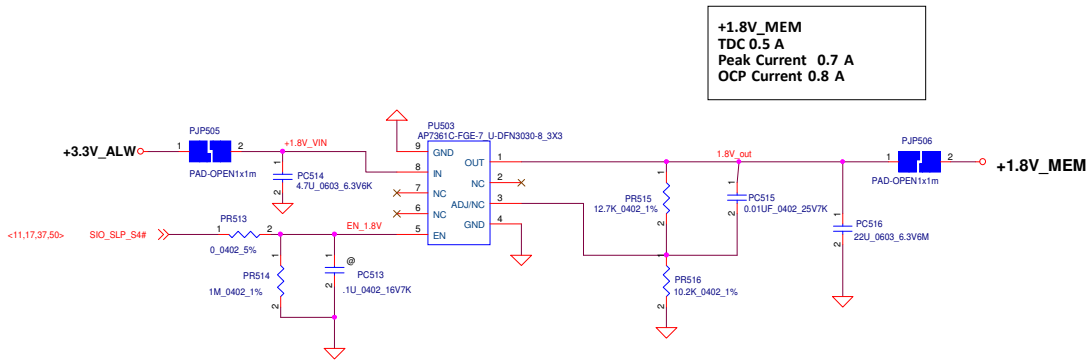

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Compal Electronics, Inc.		
Title: +1.8VALWP/1.8V_MEN		
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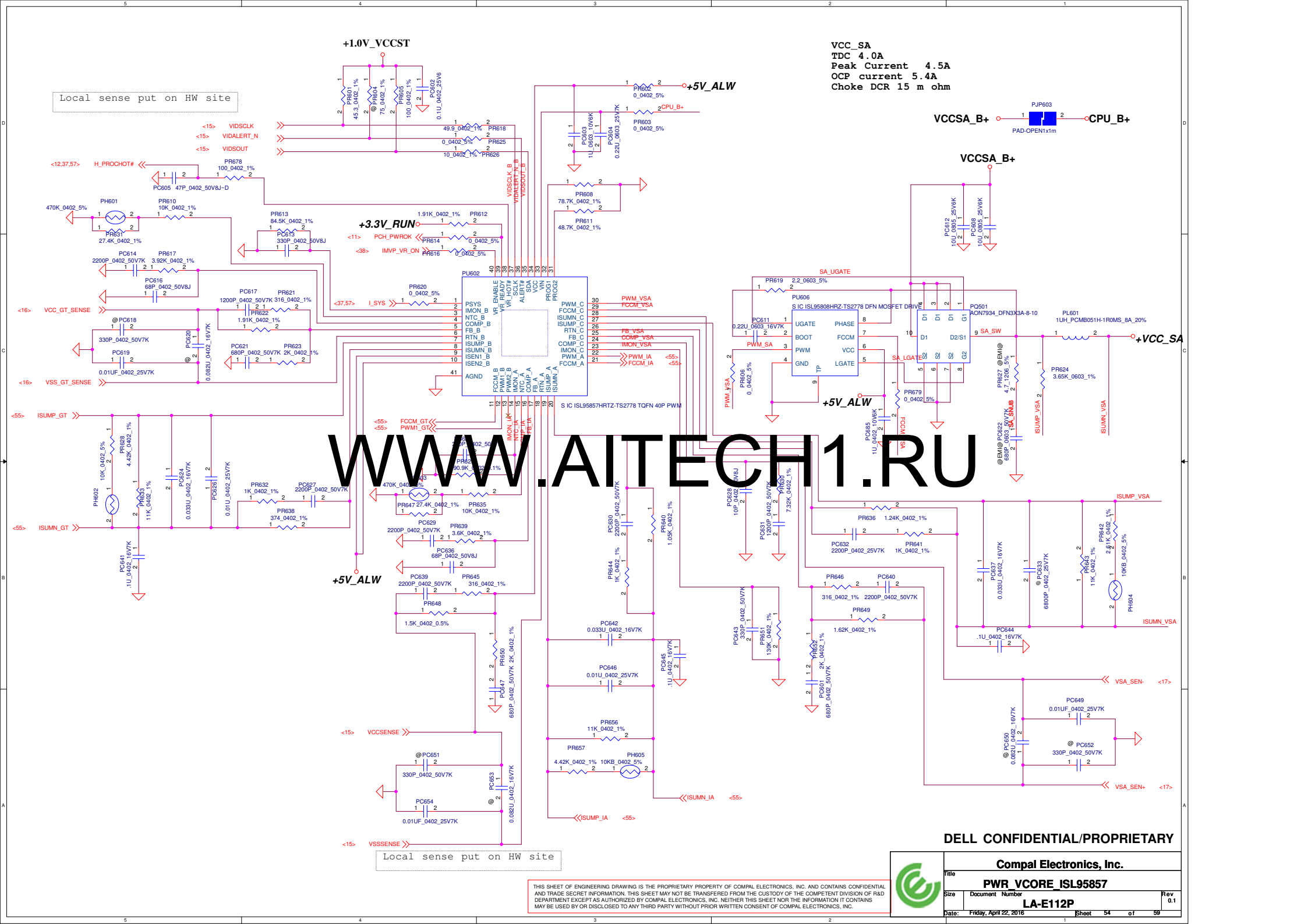

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Compal Electronics, Inc.	
Title	PWR_VCORE_ISL95857
Size	Document Number: LA-E112P
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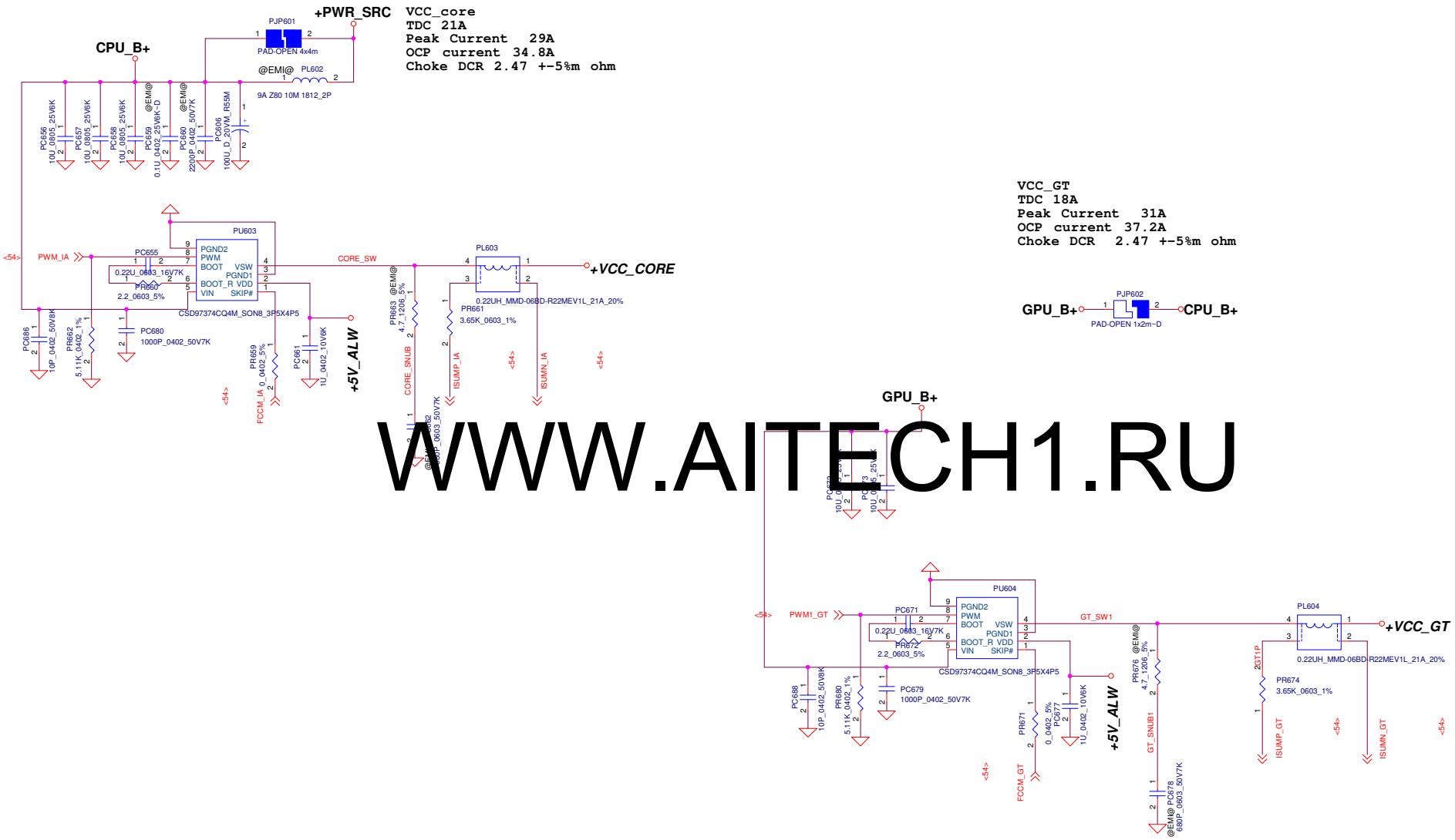
Date: Friday, April 22, 2016	Sheet 54 of 59



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Compal Electronics, Inc.	
Title	PWR_VCORE_ISL95857
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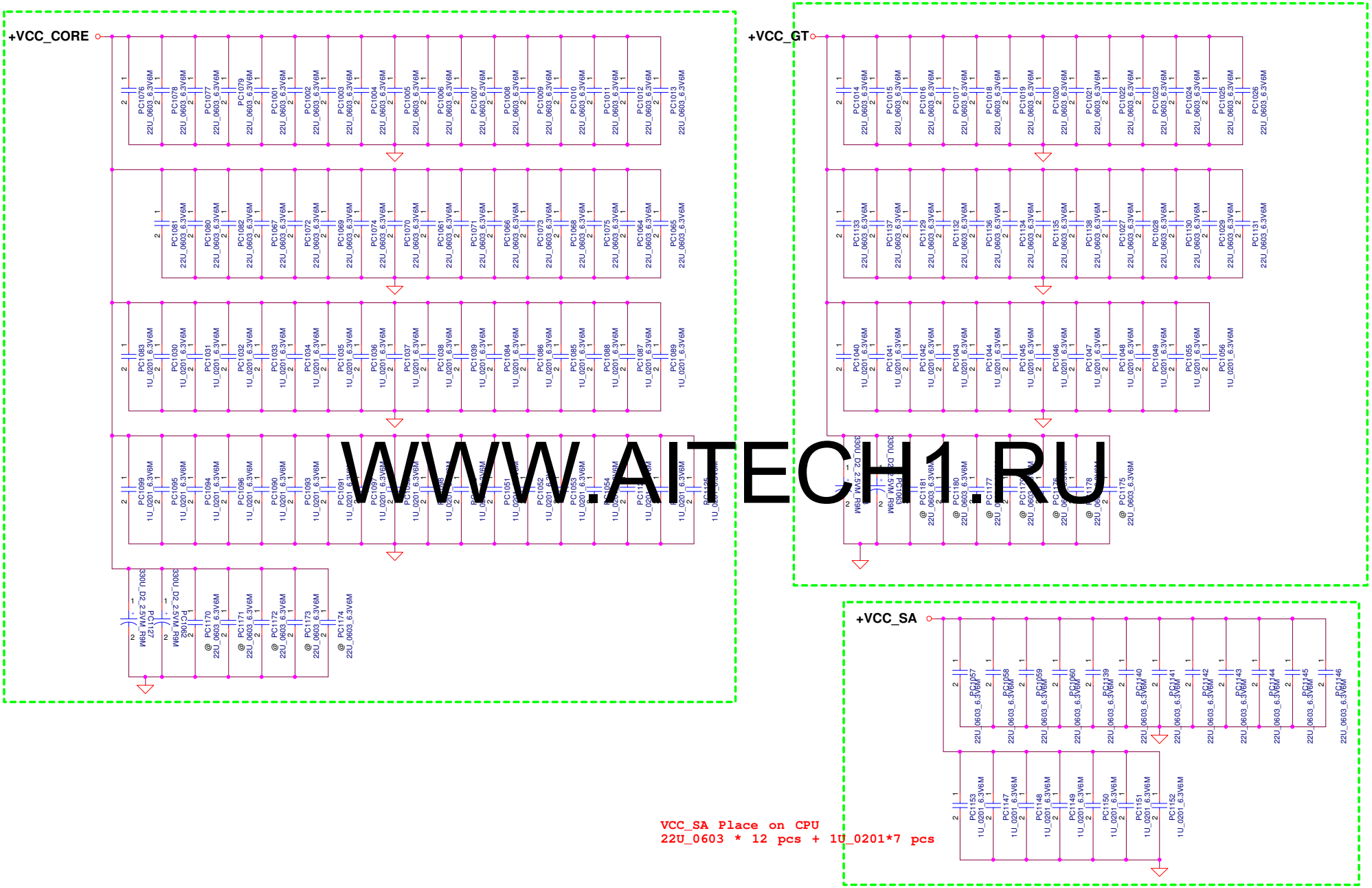
VCC_CORE Place on CPU
22U_0603 * 33 pcs +1U_0201*35 pcs
+330u_D2*2 pcs

VCC_GT Place on CPU (U22)
22U_0603 * 26 pcs +1U_0201*12 pcs
+330u_D2*2 pcs

VCC_GT Place on CPU (U23E)
22U_0603 * 48 pcs +1U_0201*12 pcs
+330u_D2*3 pcs



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VCC_SA Place on CPU
22U_0603 * 12 pcs + 1U_0201*7 pcs

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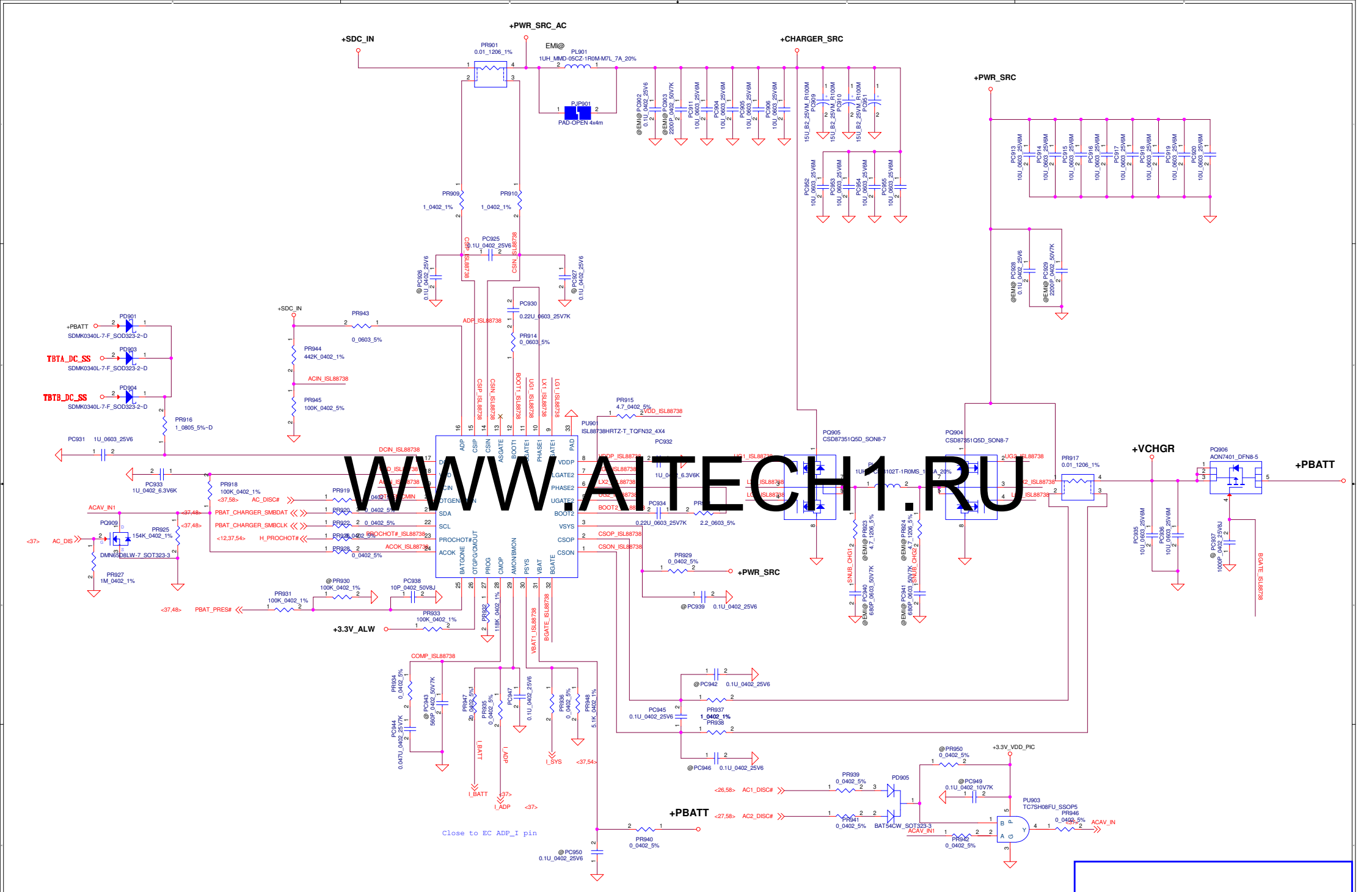
Compal Electronics, Inc.	
Title	PROCESSOR DECOUPLING
Size / Document Number	LA-E112P
Rev	0.1
Date: Friday, April 22, 2016	Sheet 56 of 59



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Security Classification	Compal Secret Data		
Issued Date	2014/10/24	Deciphered Date	2015/08/31

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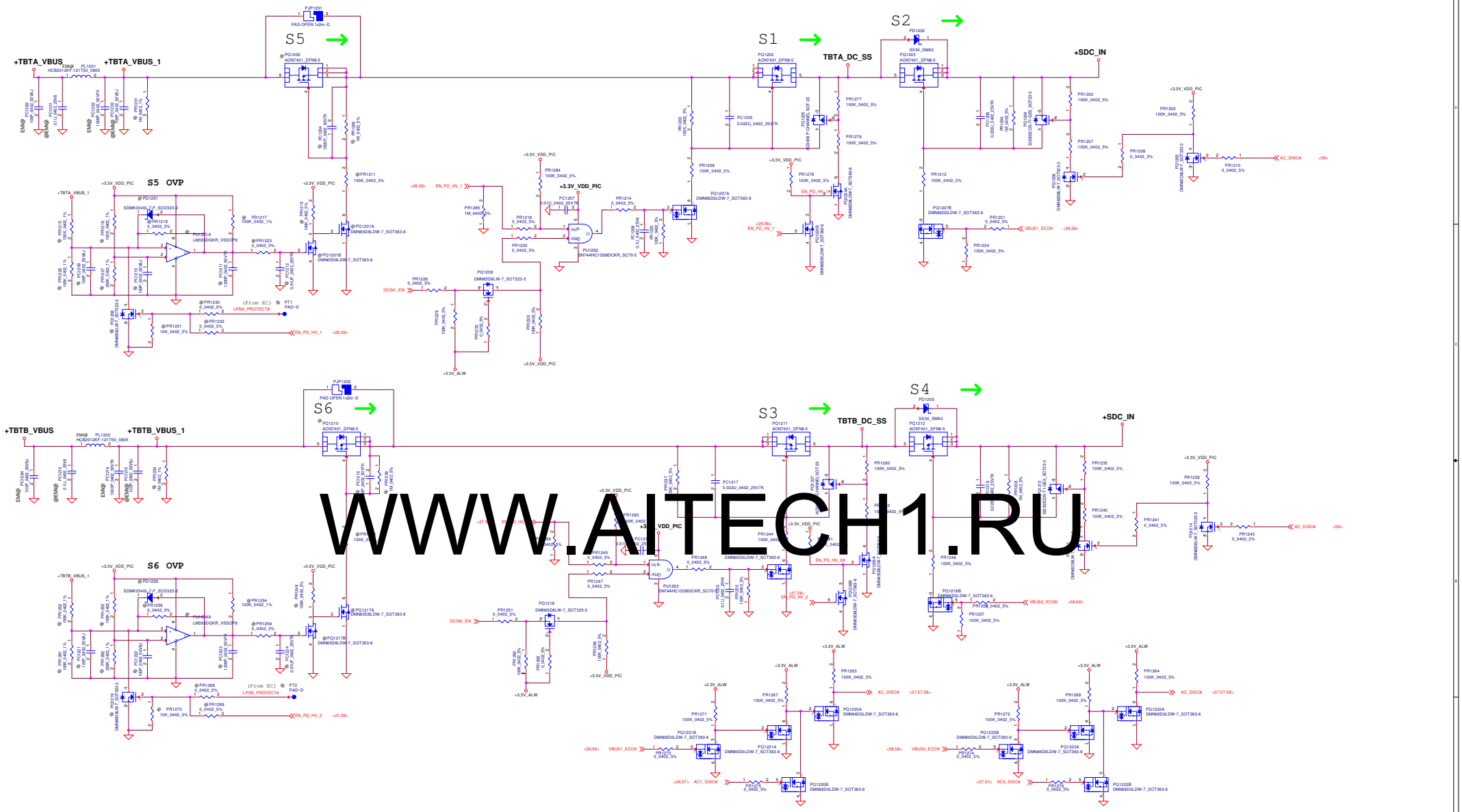
Compal Electronics, Inc.

Title: **P47-PWR CHARGER ISL9237 (Colay)**

Size: | Document Number: **LA-E112P** | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 57 of 59



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Security Classification	Compal Secret Data		
Issued Date	2015/06/10	Deciphered Date	2015/06/10

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Compal Electronics, Inc.

Title: **P51 - PWR DCIN/BATT CONN/OTP**

Size: | Document Number: **LA-E112P** | Rev: 0.1

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	55	1.8VALW/+1.2V/ 1.8V_MEN	2016 02/23	Compal	New add 1.2V_RUN (From 3.3V_RUN) by use power regulator SW ,only for HDMI PS8407 EE request	modify power rail PU502, change PR508 from 8.87K to 5.1K	X00
2	55	1.8VALW/+1.2V/ 1.8V_MEN	2016 02/23	Compal	For LPDDR3 power , add +1.8v_MEM	modify power rail PU503, change PR515 from 21.5K to 12.7K	X00
3	55	1.8VALW/+1.2V/ 1.8V_MEN	2016 02/23	Compal	PU501 PG connect to +1.8V_RPIM_PWRGD & Pull high to 3.3V	modify power rail PU501, pull high to 3.3V and connect netname +1.8V_PRIM_PWRGD	X00
4	55	1.8VALW/+1.2V/ 1.8V_MEN	2016 03/01	Compal	HW dropped PS8407 solution.	Remove 1.2V_RUN (PU502) power rail.	X00
5	52	+1.2V_MEM/ +0.6V_DDR	2016 03/07	Compal	remove 1.2V_DDR_PG	remove 1.2V_DDR_PG,remove PR201	X00
6	60	1Type-C PD Selector	2016 03/17	Compal	to add S4 quick turn off 3/14 by chris	add PQ1224 PQ1225 PQ1226 PQ1227	X00
7	60	1Type-C PD Selector	2016 03/23	Compal	EMI request	add PR1283 PR1284	X00
8							
9							
10							
11							
12							
13							
14							

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